A SWITCHED CAPACITOR ADAPTIVE LINE EQUALIZER FOR A HIGH-SPEED DIGITAL SUBSCRIBER LOOP

Yoshiaki KURAISHI, Yutaka TAKAHASHI, Kenji NAKAYAMA and Takashi SENBA*

Transmission Div., *System LSI Development Div., NEC Corporation
Kawasaki-City, 211 JAPAN

ABSTRACT

A single-chip adaptive line equalizer system which is used for high-speed (200 kb/s) digital subscriber loops is presented. The equalizer system mainly consists of a pre-filter, a $\sqrt{f}$ equalizer (EQL), a rolloff filter, a post-filter, a level detector and a control circuit. The $\sqrt{f}$ EQL is further divided into a coarse $\sqrt{f}$ EQL and a fine flat EQL. Switched capacitor network technology is successfully applied to synthesizing the filters and the $\sqrt{f}$ EQL which have to operate at high sampling rates on monolithic MOS circuits. An efficient approach to designing the SC $\sqrt{f}$ EQL is proposed, which can decrease a total amount of capacitors. In order to realize high-speed operational amplifiers, 3 μm CMOS technology is employed. The analog section including the filters and the $\sqrt{f}$ EQL occupies 5 mm^2 of chip area, and has a power consumption of 94 mW with a 5 V single power supply. Eye openings of 90 percent are obtained from the experimental results.

INTRODUCTION

With recent advancement in various digital transmission networks, there exist a great demand for digital high-speed bidirectional transmission system utilizing analog subscriber loops [1]. In order to achieve high performance digital subscriber transmission systems economically and in small size, integration of an adaptive line equalizer ($\sqrt{f}$ EQL) system is an important technical objective. Switched capacitor network technology has been applied to implementing the adaptive $\sqrt{f}$ EQL system operating at a high sampling frequency on monolithic MOS circuits [2], [3].

This paper presents a single-chip adaptive line equalizer system applied to high-speed (200 kb/s) digital subscriber loops. This paper places stress on the design of a switched capacitor adaptive $\sqrt{f}$ EQL, which is directed toward reductions in a total amount of capacitors, and consequently in chip area and power consumption. Furthermore, efficient algorithms for controlling an adaptive $\sqrt{f}$ EQL and a bridged tap equalizer are provided. Monolithic MOS circuit implementation using 3 μm CMOS technology is also presented.

SYSTEM DESCRIPTION

A system configuration for the digital subscriber loop is briefly given in Fig. 1. The bipolar coded 200 kb/s signal is bidirectionally transmitted through a twisted pair cable in a burst mode. Therefore, the equalizer system alternately operates as a transmitter and a receiver. A block diagram for the adaptive line equalizer system is illustrated in Fig. 2. The pre-filter is used for anti-aliasing. Line loss characteristics are equalized by the $\sqrt{f}$ EQL. The transmitted rectangular pulses (50 % duty) are shaped through the rolloff filter so as to minimize intersymbol interference, in other words, maximize eye openings. The rolloff output signal having a sampled and hold wave form is smoothed by suppressing high frequency components through the analog post-filter. Echo pulses reflected from bridged taps are cancelled through the bridged tap equalizer. The peak value of the output is measured by the detector and is used for generating the control signal for the adaptive $\sqrt{f}$ EQL.

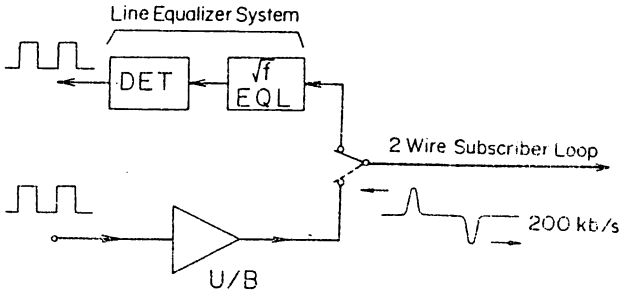

Fig. 1. Digital subscriber loop.

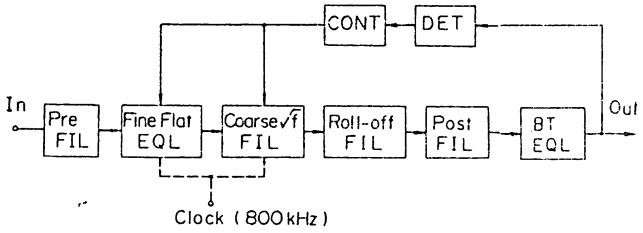

Fig. 2. Adaptive line equalizer system.

The pre- and post-filters are basically synthesized with analog circuits such as RC active filters. However, such analog filters usually occupy a large area on monolithic MOS circuits. Therefore, it is desirable to synthesize these filters in a mixed form of analog and sampled-data filters [4].

The $\sqrt{f}$ EQL consists of a coarse $\sqrt{f}$ EQL and a fine flat EQL, and is automatically controlled so as to adjust gain from 0 to 45 dB at the Nyquist frequency (100 kHz). The line loss characteristics are mainly equalized by the coarse $\sqrt{f}$ EQL and the fine flat EQL is used for adjusting the gain difference between the adjoining coarse $\sqrt{f}$ EQL step responses. Both the equalizers have 16 step responses, then the $\sqrt{f}$ EQL has 256 step responses as a whole, and can adjust gain at the Nyquist frequency by 0.2 dB.

DESIGN OF $\sqrt{f}$ EQL

Sampling Frequency

A sampling frequency is one of important parameters which determine a dynamic range of capacitor values in SC networks and circuit size of the anti-aliasing and smoothing filters. Since high speed operation and a wide range of gain control are required for the $\sqrt{f}$ EQL, the former condition seems to be dominant. For this reason, the sampling frequency is determined to four times as high as the input data rate 200 kHz, that is 800 kHz.

Transfer Function Approximation

In the data transmission systems, transmission quality can be evaluated by an error rate in terms of a signal-to-noise ratio which is equivalently the intersymbol interference (ISI). Therefore, the coarse $\sqrt{f}$ EQL transfer function is approximated by a nonlinear method in a time domain so as to minimize ISI of the time response obtained by transmitting the rectangular pulse of 50 percent duty through a system combining the transmission line, the $\sqrt{f}$ EQL and the several kinds of filters.

An example of the line frequency responses, which is the maximum loss 45 dB at the Nyquist frequency, is illustrated in Fig. 3. The optimum pole-zero

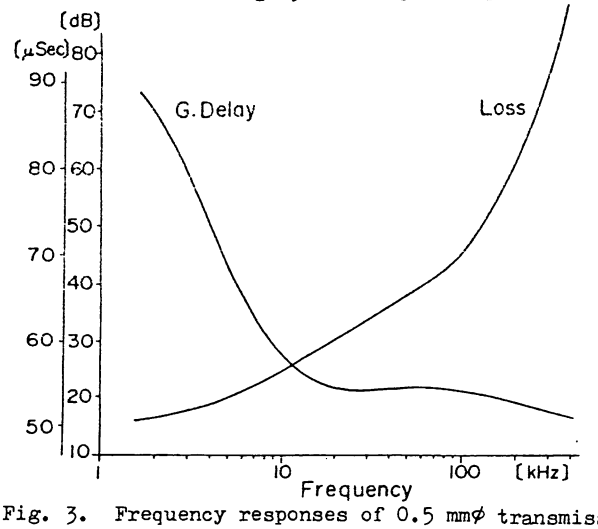

Fig. 3. Frequency responses of 0.5 mmφ transmission line with the maximum loss 45 dB at the Nyquist frequency 100 kHz.

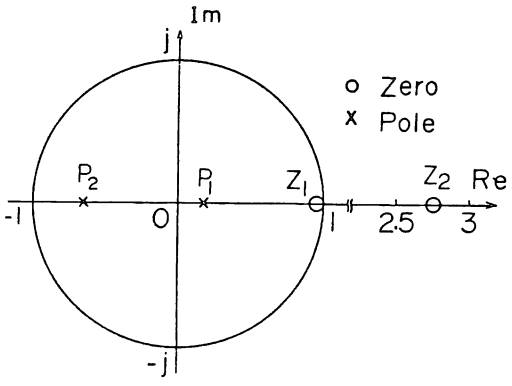

Fig. 4. Pole-zero location of coarse $\sqrt{f}$ EQL.

locations to equalize the line characteristic are given in Fig. 4. The line amplitude and group delay responses are mainly equalized using Z_1. P_1 and Z_2 are used for further compensating the line amplitude and group delay responses in the low and middle frequency bands. Furthermore, P_2 located on the negative real axis is used for shaping the amplitude response in the high frequency band.

SC Biquad Structure

The E circuit among a family of SC biquads reported in [5] is selected to realize the 2nd-order coarse $\sqrt{f}$ EQL transfer function having the poles and zeros shown in Fig. 4. The circuit configuration is shown in Fig. 5. Since the coarse $\sqrt{f}$ EQL realize 16 step responses, the variable capacitor to which an arrow is attached has 16 kinds of values, and one of them is selected to realize a desired response.

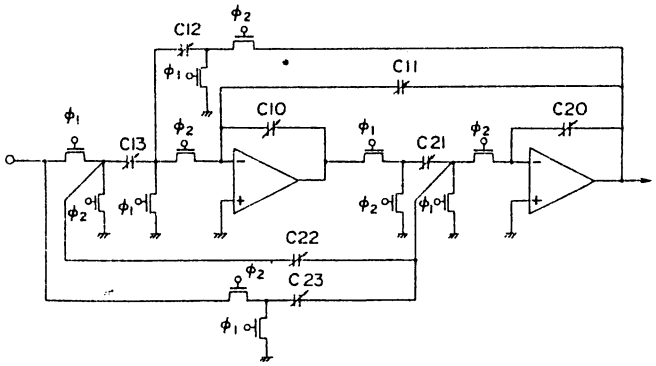

Fig. 5. Circuit configuration for coarse $\sqrt{f}$ EQL.

The capacitor values are rounded off into integer values in order to attain high accuracy capacitor ratios with a small unit capacitor, at the same time, to make simple capacitor value control possible.

Fine Flat EQL

Since the $\sqrt{f}$ EQL response is discretely changed, group delay time differences between the adjoining coarse $\sqrt{f}$ EQL step responses exist. When this delay time difference is not neglected, it affects as timing jitter and degrades the error rate performance of the data transmission systems. The fine flat EQL

is also utilized for compensating the delay time differences. The circuit configuration is shown in Fig. 6, which has a pole on the positive real axis. The fine flat EQL has three kinds of poles, in other words, three groups of frequency responses, as shown in Fig. 7, in order to gradually vary group delay time.

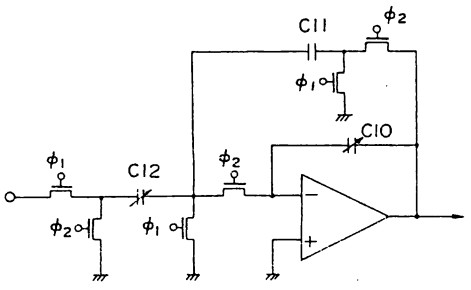

Fig. 6. Circuit configuration for fine flat EQL.

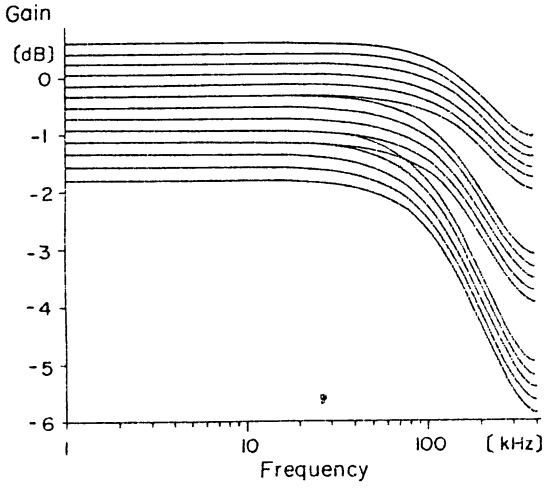

Fig. 7. Fine flat EQL amplitude responses in dB.

Calculated Performances

Figure 8 shows the overall amplitude responses in dB including the filters and the $\sqrt{f}$ EQL. Eye openings of 80 percent and 90 percent without and with the bridged tap equalizer [6] are obtained, respectively. The maximum delay time difference 0.34 μsec, which is 6.8 percent of 5 μsec (=1/200 kHz), between the adjoining coarse $\sqrt{f}$ EQL step responses is reduced to 0.14 μsec by the fine flat EQL.

DESIGN OF OTHER BLOCKS

Adaptive $\sqrt{f}$ EQL Controller

An adaptive $\sqrt{f}$ EQL controller consists of a counter control circuit, an up/down counter, a programmable logic array (PLA) and a latch circuit as shown in Fig. 9. The counter control circuit produces pulses to be counted by the up/down counter.

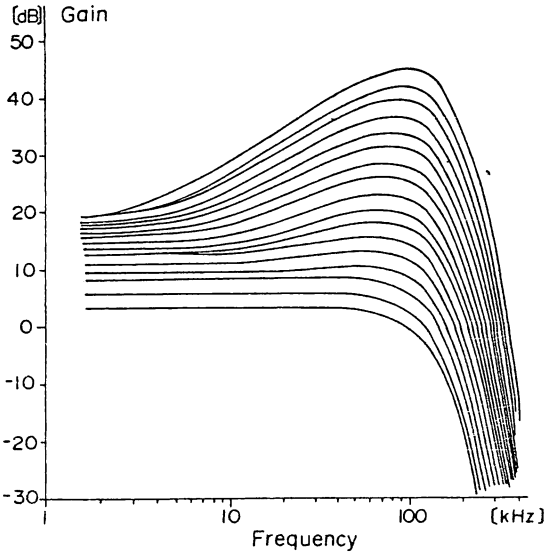

Fig. 8. Amplitude responses in dB for an overall system including the filters and the $\sqrt{f}$ EQL.

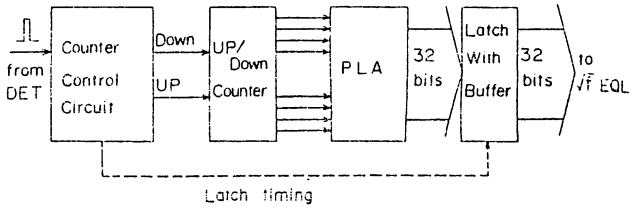

Fig. 9. Block diagram for adaptive $\sqrt{f}$ EQL controller.

When the peak level detector input voltage is larger or smaller than the reference voltage, the pulse is counted down or up, respectively. The counter controller has two operating modes. One of them is a high speed counting mode, where the counter control pulse is generated for each detector output pulse. The other is a low speed counting mode, where the counter control pulse is generated after integrating the detector output pulses for a some time period. This mode provides stable gain control, in other words, the $\sqrt{f}$ EQL gain control does not suffer from an impulse noise.

The adaptive $\sqrt{f}$ EQL step response starts from the maximum gain step and reaches the appropriate step response having the gain corresponding to the actually laid transmission line length, through the high speed counting mode during the period of the $\sqrt{f}$ EQL training. The counter control mode is automatically changed from the high speed mode to the low speed mode after the $\sqrt{f}$ EQL step response settles down. These two counting modes can accomplish a very fast $\sqrt{f}$ EQL training, at the same time, stable gain control in data transmission.

The up/down counter output has an 8 bit parallel code. The high and low significant 4 bits are assigned to controlling the coarse $\sqrt{f}$ EQL and the fine flat EQL, respectively.

Bridged Tap Equalizer

Bridged taps in the digital subscriber loops reflect the transmitted pulses and cause the echo pulses appear after the main pulse. These echo pulses usually have large amplitude and serious eye opening degradation results. Therefore, echo pulse cancellation is one of important functions for the line equalizer system. The developed 2nd-order bridged tap equalizer having a decision feedback is illustrated in Fig. 10. The data detector consists

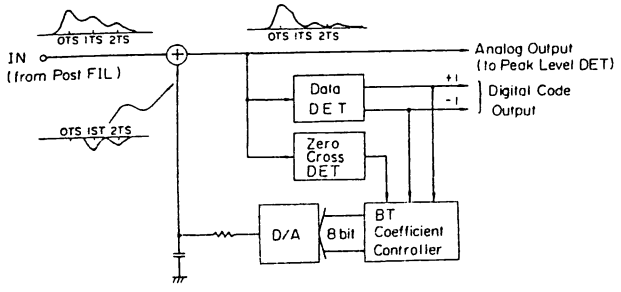

Fig. 10. Block diagram for 2nd-order bridged tap equalizer.

of two comparators and descriminates the received bipolar signals (+1, -1). The zero cross detector includes a comparator, and produces a wave form having amplitude of positive constant or zero according to the polarity of the input signal which is positive or negative, respectively. The coefficient controller generates the BT EQL coefficients and stores them, furthermore, controls the coefficient output timing. The residual echo pulses are sampled at one and two time slots after the main pulse when the specific bit stream of 0100 is observed by the data detector. The coefficients having an 8 bit digital code are increased or decreased according to the polarity of the residual echo pulses. The 8 bit digital code is converted into a rectangular pulse by the D/A converter. The pulse is shaped to a triangular wave form by a 1st-order CR filter and is cancelled by the adder.

One of the features for the proposed BT EQL is to reduce a power consumption by using digital control circuits. The other is to accomplish high tap gain control such as over 70 and 50 percent echo cancellation at one and two time slots after the main pulse. Furthermore, the BT EQL can effectively suppresses the relatively large intersymbol interference caused by using different kinds of transmission lines from the typical which is used for the $\sqrt{f}$ EQL design.

DC Offset Canceller

In SC systems, dc offset voltages appearing in the output signal are caused by amplifier input offsets and clock feedthrough. The output offsets are not neglected comparing the reference voltage 0.5 V_{op} for the post-filter output, and narrow the eye openings. In order to eliminate the output offsets, an offset canceller is employed at the post-filter output. The output offsets are measured and stored in a capacitor during the equalizer system operates as a transmitter, by connecting the input terminal of the pre-filter to the analog ground. The measured offsets are subtracted from the post-filter output by an SC subtractor in the receiving mode.

MONOLITHIC MOS IMPLEMENTATION

Operational Amplifier

Since the clock rate of the $\sqrt{f}$ EQL is 800 kHz, and that of the other SC filters is chosen to be higher than 800 kHz in order to simplify the RC active filter circuits, high-speed operational amplifiers must be realized on monolithic MOS circuits. For this purpose, and to make a whole chip area small, 3 μm CMOS technology is employed. The operational amplifier having the following high performances was designed. They include an loop gain of 72 dB, an unity gain frequency of 14 MHz and a settling time of 160 nsec for 1.0 percent settling down with the maximum capacitive load of 38 pF.

Variable Capacitor

A reduction in capacitors is a very important design objective in the SC circuit implementation to achieve high speed operation with a small power consumption and a small chip area. Since all capacitor values in the SC circuits are rounded off into integer values as described previously, and can be synthesized using the plural number of the same unit capacitors, edging error effects on capacitor ratios are very small. This means a small unit capacitor can be employed to obtain desired filter performances. In the developed SC circuits the unit capacitor value is chosen to be 0.2 pF having an area of 225 μm^2.

The variable capacitor is constructed as a programmable capacitor array as show in Fig. 11. The branch capacitors are also synthesized using the plural number of the unit capacitors. Appropriate branch capacitors are selected through the switches to realize the desired capacitor in a parallel form.

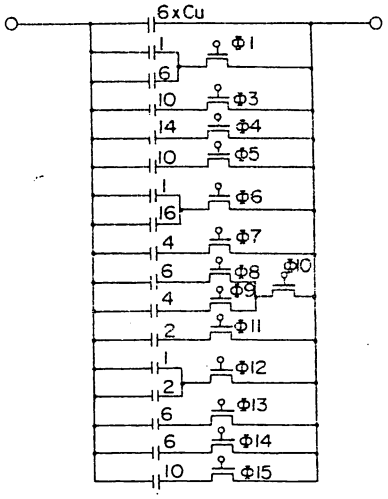

Fig. 11. Programmable capacitor array used for variable capacitors.

Fabrication

The adaptive line equalizer system was fabricated as an integrated circuit using the 3 μm CMOS technology. A chip photograph of the analog section including the filters and the $\sqrt{f}$ EQL is given in Fig. 12. The area and power consumption of the analog section are about 5 mm^2 and 94 mW with a 5 V single power supply, respectively.

From the experimental results, it was confirmed that the calculated performances of the equalizer system are mostly realized through the monolithic CMOS circuit implementation. One of the measured eye openings is shown in Fig. 13.

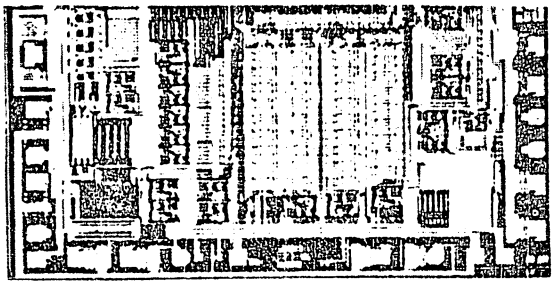

Fig. 12. Chip photograph of the analog section.

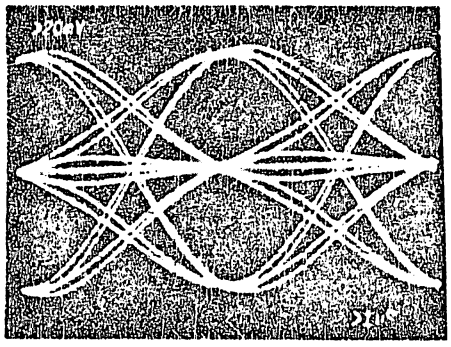

Fig. 13. Measured eye pattern for 0.5 mmϕ transmission line.

CONCLUSION

Through newly introduced design techniques, such as time domain approximation of the $\sqrt{f}$ EQL transfer function, operational amplifier design with the 3 μm CMOS technology and efficient algorithms for controlling the $\sqrt{f}$ EQL and the bridged tap equalizer, the high-speed switched capacitor adaptive line equalizer system providing high eye opening rates was accomplished on a monolithic integrated circuit with a low power consumption and a small chip area. The LSI equalizer system is now successfully applied to the high-speed (200 kb/s) digital transmission systems.

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