24- AND 120-CHANNEL TRANSMULTIPLEXERS BUILT WITH NEW DIGITAL SIGNAL PROCESSING LSI'S

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Reprinted from IEEE Transactions on Communications, Vol. COM-30, No. 7, July 1982
0090-6778/82/0700-1528$00.75

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Abstract—**Two new digital transmultiplexers intended for commercial use have been developed. One transmultiplexer performs a bilateral conversion between two 12-channel FDM group signals and a 24-channel PCM carrier signal. The other mutually connects two 60-channel FDM supergroup signals and five 24-channel or four 30-channel PCM signals. Both exploit a block processing digital SSB-FDM multiplex/demultiplex scheme employing a cascade of an FFT processor and a set of complex coefficient digital filters. They have been built using newly developed high-level DSP LSI chips. Algorithmic considerations, developed LSI architecture, and equipment configuration are described as well as digital processor design details and measured performance.**

I. INTRODUCTION

THE need for TDM/FDM conversion is growing rapidly as new digital communication systems are introduced within existing analog telecommunication networks. The "transmultiplexer," which performs the conversion, has attracted much attention among engineers who consider the application of digital signal processing (DSP) techniques. Various ingenious and extensive reports have been published on the DSP technique exploitation for transmultiplexer realization, establishing a mature theoretical base [1]-[13]. Some hardware models have been actually developed, and satisfactory transmission performance as well as the inherent accuracy and stability of the all-digital design have been demonstrated [5], [7], [12]-[14].

Despite the situation, digital transmultiplexers have not gained much popularity in actual networks so far. This is because the hardware techniques to implement the developed DSP algorithms have not reached a very mature level as yet, especially in regard to cost, size, and power consumption requirements. Hence, in the area where introduction of digital time division switches started early, analog transmultiplexers based on conventional per-channel technology have been developed and put into service to satisfy the urgent demand for efficient TDM/FDM conversion [15]-[18].

However, it is anticipated, from the potential merits of DSP techniques, that the digital approach would be eventually employed. Thus, algorithmic and implementational improvements have still been pursued very actively [19]. One encouraging factor that can be counted on to aid new developmental work is the progress in state-of-the-art VLSI technology that has appeared in the last few years. Although the need for multipliers has been a burden on hardware designers up to a few years ago, the present day LSI chips can accommodate several multipliers together with other logic and memory elements in a single die area [21], thereby enabling formation of more effective and higher level DSP functional blocks than such elementary functional units as an adder, a subtractor, and a multiplier.

This paper describes two new digital transmultiplexers intended for commercial use. One is a 24-channel transmultiplexer that performs a bilateral conversion between two 12-channel FDM group signals (2 × FDM BG) in the 60-108 kHz band and a 24-channel PCM carrier signal at 1.544 Mbits/s. The other is a 120-channel transmultiplexer that converts two 60-channel FDM supergroup signals (2 × FDM BSG) in the 312-552 kHz band into five 24-channel PCM signals or four 30-channel PCM signals at 2.048 Mbits/s, and vice versa. As far as the ease of gaining digital implementation merits is concerned, conversion at the supergroup level is more effective. However, in countries where 24-channel PCM carrier systems are widespread, there are also opportunities for interfacing at the group level.

Both transmultiplexers have been built using a "high-level DSP chip set" that has been newly developed [22] to reduce size, cost, and power consumption for digital transmultiplexers, so that they can be competitive with conventional analog counterparts.

Algorithmic considerations, developed DSP LSI architecture, equipment configurations, and design parameters are presented, as well as digital processor design details and measured performance.

II. CONVERSION ALGORITHM

Both 24- and 120-channel transmultiplexers are based on the same algorithm previously proposed [6]. The algorithm is characterized by use of a cascade of a K-point FFT processor and a set of K complex coefficient filters, for multiplexing K real baseband sequences at an 8 kHz rate into an SSB-FDM sequence at an 8 × K kHz rate. The FFT processor and the digital filters both operate at 8 kHz rate.

Denoting Z transforms of K baseband sequences and an SSB-FDM sequence as $\{X_k(Z^K)\}$; $(k = 0, 1, \cdots, K-1)$ and $Y(Z)$, respectively, the multiplexing process can be described

Manuscript received June 14, 1981; revised November 10, 1981. This paper was presented in part at the International Conference on Communications, Denver, CO, June 15-18, 1981.

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0090-6778/82/0700-1528$00.75

by the following expressions [6]:

$$Y(Z) = \sum_{i=0}^{K-1} 2 \cdot Z^{-i} \cdot \mathrm{Re}\,\{G_i(-jZ^K) \cdot A_i(Z^K)\} \tag{1a}$$

$$A_i(Z^K) = \sum_{k=0}^{K-1} \tilde{X}_k(Z^K) \cdot \exp\{j2\pi(4k+1)i/4K\} \tag{1b}$$

where

$$\tilde{X}_k(Z^K) = X_k(Z^K), \quad \text{for } 0 \leqslant k \leqslant K/2 - 1$$
$$= X_k(-Z^K), \quad \text{for } K/2 \leqslant k \leqslant K - 1$$

and $G_i(-jZ^K)$ is the Z-transfer function of the ith subfilter in a set of K complex coefficient filters constituting a "polyphase network." The operator Re $\{\cdot\}$ in (1a) denotes that only the real part of the time sequence for $\{\cdot\}$ is to be retained. From a similarity to the discrete Fourier transform (DFT), (1b) can be efficiently calculated by using a K-point FFT processor. Thus, the structure for realizing the multiplexing process, based on the above equations, becomes as shown in Fig. 1(a).

Similarly, the demultiplexing process is described by the following equations:

$$\tilde{X}_k(Z^K) = 2 \cdot \mathrm{Re}\left(\sum_{i=0}^{K-1} B_i(Z^K) \cdot \exp\{j2\pi(4k+1)i/4K\}\right), \quad 0 \leqslant k \leqslant K-1 \tag{2a}$$

$$B_i(Z^K) = G_i(-jZ^K) \cdot Y_{K-1-i}(Z^K) \tag{2b}$$

where $\{Y_{K-1-i}(Z^K)\}$; $(i = 0, 1, \cdots, K-1)$ are subsampled sequences of $Y(Z)$ and satisfy the relation

$$Y(Z) = \sum_{i=0}^{K-1} Z^{-i} \cdot Y_{K-1-i}(Z^K). \tag{3}$$

Fig. 1(b) shows a block diagram for realizing the demultiplexing process.

In order that the configurations shown in Fig. 1(a) and (b) properly function as the SSB-FDM modulator and demodulator, a set of filters with transfer functions $\{G_i(-jZ^K)\}$; $(i = 0, 1, \cdots, K-1)$ must have certain amplitude and phase relationships. This requirement is automatically satisfied by deriving $\{G_i(-jZ^K)\}$; $(i = 0, 1, \cdots, K-1)$ from a single real coefficient low-pass filter with transfer function $G(Z)$ operating at $8 \times K$ kHz rate, according to the following procedures.

1) Design $G(Z)$ so that it has a half bandwidth of the required SSB signal passband, and satisfies all the frequency response requirements, such as in-band ripple, group delay distortion, and out-of-band loss for crosstalk attenuation.

2) Derive a set of K transfer functions $\{G_i(Z^K)\}$; $(i = 0, 1, \cdots, K-1)$ from $G(Z)$ so as to satisfy the relation

$$G(Z) = \sum_{i=0}^{K-1} Z^{-i} \cdot G_i(Z^K). \tag{4}$$

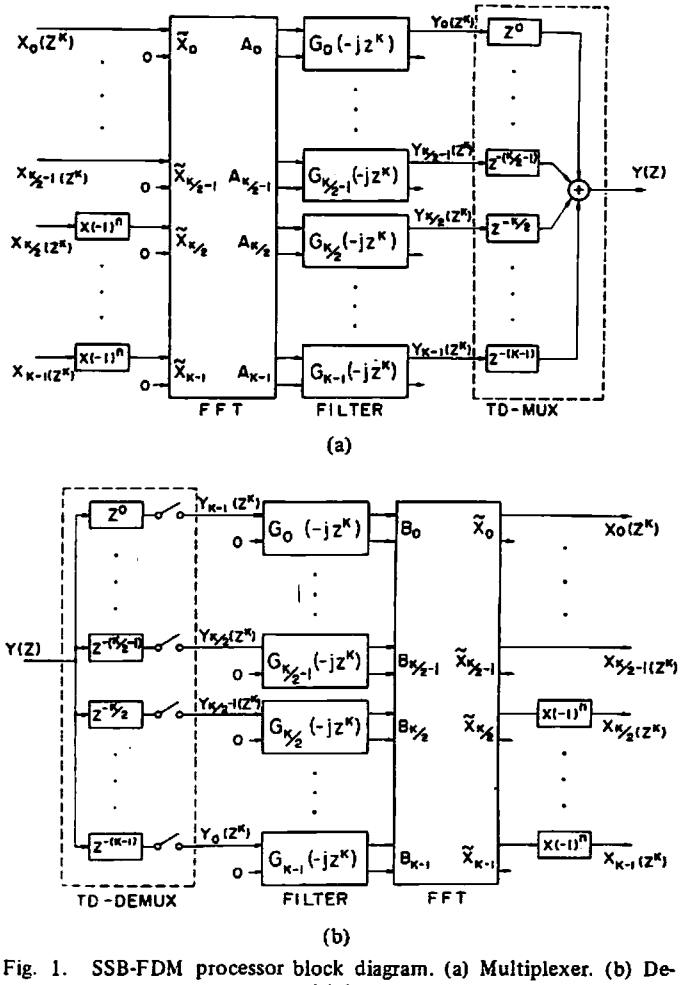


Fig. 1. SSB-FDM processor block diagram. (a) Multiplexer. (b) Demultiplexer.

The magnitude responses of all $G_i(Z^K)$ thus derived are identical to each other as well as to the magnitude response of $G(Z)$ within a −4 to 4 kHz range, and the phase difference between $G_i(Z^K)$ and $G_0(Z^K)$ is linear in the passband with slope $(2\pi i/K)$.

3) Obtain $\{G_i(-jZ^K)\}$; $(i = 0, 1, \cdots, K-1)$ by substituting $-jZ^K$ for Z^K in $\{G_i(Z^K)\}$; $(i = 0, 1, \cdots, K-1)$. By this substitution, the coefficients of the odd power of Z^K in the transfer function become purely imaginary and those of the even power of Z^K remain purely real, thereby having effect in a 2 kHz shift along with the frequency axis.

As can be seen from Fig. 1(a), the input to the FFT processor is limited to real signals and only the real part of the complex output from the filter is needed in the multiplexer. Also, in the demultiplexer, the input to the filters is limited to real, and only the real component is required at the FFT outputs. These properties can be utilized to reduce the number of multiplications required per channel and per second.

For example, the FFT processor multiplication rate can be halved by either 1) sharing a single processor between two independent sets of signals [6] as used in the 120-channel transmultiplexers [13], [14], 2) using a $K/2$ point FFT processor with an auxiliary processor [11] as used in the 60-channel transmultiplexer [20], or 3) using a DCT (discrete cosine transform) calculator, as will be described in Section

V for application to the 24-channel transmultiplexer. The multiplication rate for a set of digital filters can also be halved if the Z-transfer function $G(Z)$ is designed so that it has a numerator polynomial $N(Z)$ with symmetric coefficients and denominator polynomial $D(Z^{2K})$ which is only a function of Z^{2K}, and if a special direct-form implementation is employed [10], [20].

These multiplication rate reduction techniques were proven to be useful in minimizing hardware size and cost in previous referenced developments. However, their degree of significance has gradually been reduced as the LSI/VLSI technology advances, thus requiring total hardware simplicity pursuit rather than a minimum multiplication rate achievement. In other words, a straightforward implementation with VLSI chips could often be simpler and more cost effective than an implementation with a reduced multiplication rate but with very special and complicated signal flows, in which VLSI chips cannot be efficiently applied. This is the case actually observed in the digital filter for the present transmultiplexer development. A straightforward complex coefficient digital filter, with some redundant calculations, was preferred to the special direct-form implementation of the filter with a halved multiplication rate.

III. DSP CHIP SET DEVELOPMENT

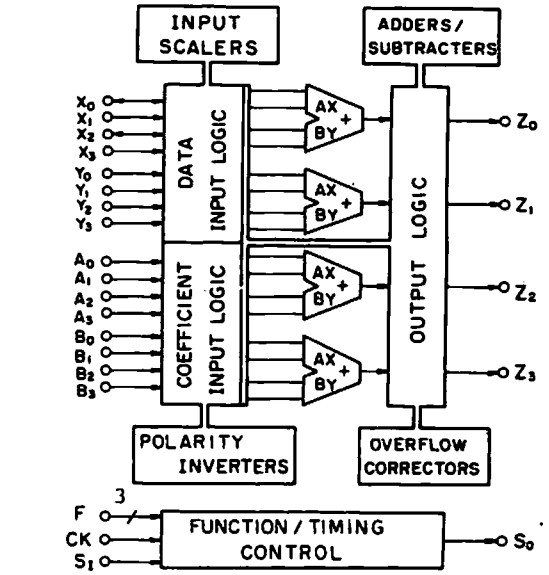
In order to reduce the total number of chips required to build a transmultiplexer, as well as to reduce power consumption, use of custom-made LSI chips, optimized for application in some specific equipment, would give the best solution. However, developing such custom-made LSI chips, solely for a transmultiplexer, cannot be justified in view of production volume, which is a prime factor for cost reduction.

Thus, a set of general purpose, high-density DSP building block elements, called a "high-level DSP chip set," has been developed [22]. The chip set consists of two LSI chips, the "arithmetic processor unit (APU)" and the "variable delay unit (VDU)." The architecture optimization has been sought so that these two chips constitute a versatile and self-sufficient DSP chip set, while keeping their package sizes as small as possible. Consequently, any specific DSP functions can be implemented using these two LSI chips. No other external logic devices are needed to implement some very popular DSP functions, such as biquad filter sections and FFT butterfly modules. Therefore, it is only necessary to arrange the chip sets literally as building blocks, according to a given functional block diagram, and provide timing signals and coefficients.

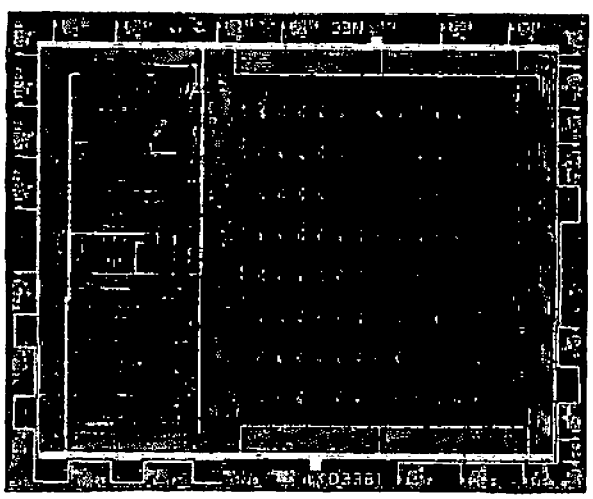
Both APU and VDU chips are single power supply, low-power Schottky TTL compatible devices. They are realized in reasonable die area (about 20 mm^2) with a proven 4.4 μm rule n-channel E/D MOS technology to guarantee high yield, high reliability, and low cost. Each chip consumes about 250 mW power, and operates at up to more than a 5 MHz clock rate.

A. Arithmetic Processor Unit (APU)

The APU is realized by integrating about 10 000 transistors in a chip, containing multipliers, adders, subtractors, and other



(a)



(b)

Fig. 2. Arithmetic processor unit (APU). (a) Block diagram. (b) Chip photomicrograph.

logic elements for such auxiliary tasks as scaling, coefficient polarity inversion, overflow correction, etc. A block diagram and a chip photomicrograph are shown in Fig. 2. The chip has eight data inputs (X_0-X_3, Y_0-Y_3), eight coefficient inputs (A_0-A_3, B_0-B_3), and four data outputs (Z_0-Z_3), each carrying a signal in serial format. The chip is mounted in a 28-pin dual-in-line package. Connections among internal functional elements and input-output pins can be altered by 3 bit function select input (F) to realize one out of eight functions listed in Table I.

Coefficient wordlength is predetermined to be 14 bits, so as to cover most requirements of a variety of telecommunication applications. However, data wordlength can be any value greater than or equal to 16 bits so that signal processing dynamic range can be arbitrarily determined depending on applications. Throughput rate is thus dependent on both clock rate and the data wordlength. Input data scaling can be made by external control within a 2^0-2^{-7} range. Coefficient polarity inversion control function is to reduce the number of stor-

TABLE I
APU FUNCTIONS

*F*0	Quadruple real $(aX + bY)$ calculators
*F*1	Dual real $\{(aX + bY) \pm (cV + dW)\}$ calculators
*F*2	Single real $\sum_{i=0}^{7} (a_i X_i)$ calculator
*F*3	Dual complex $(aX + Y)$ calculators
*F*4	Single complex $(aX + bY + W)$ calculator
*F*5	Single FFT butterfly arithmetic element
*F*6	Dual 1D biquad filter arithmetic elements
*F*7	Dual 2D biquad filter arithmetic elements

age bits for coefficients in complex number processing. Word-length is controlled by applying a sync input (S_I) pulse that indicates the least significant bit (LSB) location of the input data words. A sync output (S_O) pulse is available from the chip to indicate the LSB location of the output data words. Information for scaling and coefficient polarity control is supplied to the chip through coefficient input terminals.

B. Variable Delay Unit (VDU)

The VDU is functionally a set of four variable length shift registers, which includes an auxiliary switch. Its block diagram and its chip photomicrograph are shown in Fig. 3. Four variable shift registers are realized by a combination of RAM's and address counters. The chip integrates about 17 000 transistors in a 4.47 X 4.65 mm area. It is mountable either in a 22- or 24-pin dual-in-line package.

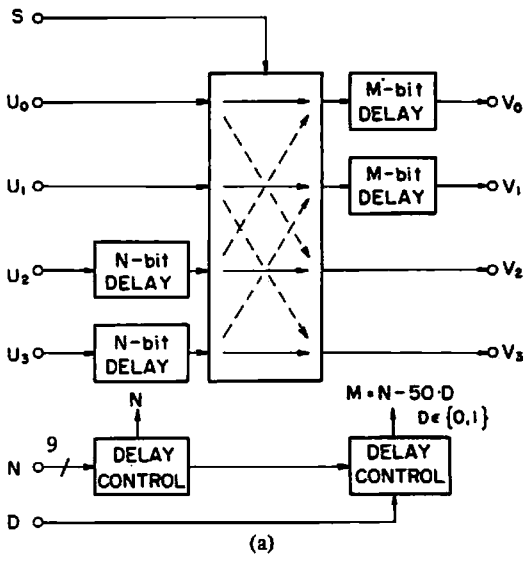
Shift register length can be varied from 8 to 519 bits with 1 bit increment externally through control terminals *N* (9 bits). By using a 1 bit control terminal *D*, the length of two shift registers can be made 50 bits shorter than that of the other two. The amount of this delay difference is equal to the total amount of delay in multipliers, adders, and overflow correctors in an APU chip for the biquad filter configuration. The built-in switch with a single control input (*S*) is aimed for time slot rearrangement required in a radix-2 pipeline FFT processor.

IV. EQUIPMENT OUTLINE

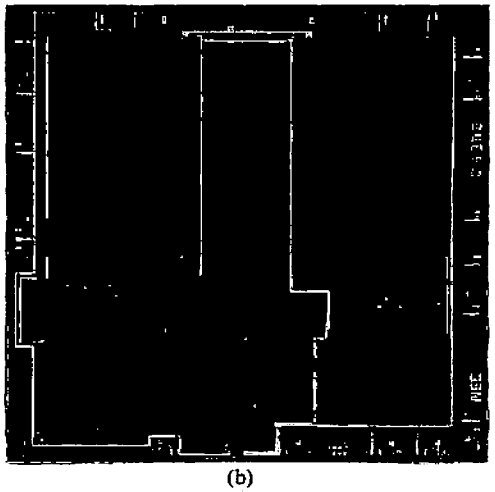
Fig. 4 shows a general block diagram common to both 24- and 120-channel transmultiplexers developed. The whole 24-channel transmultiplexer equipment is housed in a 7 in high subrack mountable in an EIA standard 19 in rack, as shown in Fig. 5(a). Fig. 5(b) shows the 120-channel transmultiplexer's digital portion housed in an $8\frac{3}{4}$ in high subrack mountable in the same rack. Another subrack of the same size is needed to constitute a whole 120-channel transmultiplexer equipment.

A. SSB-FDM Processor

This processor performs the most essential functions of the transmultiplexer: TDM-to-FDM and FDM-to-TDM conversions based on the algorithm described in Section II. In application to the group level transmultiplexer, deciding *K* to be 14 and leaving the uppermost and the lowermost channels unused, 12 baseband channels are directly multiplexed into the 60-108 kHz standard basic group band, thus eliminating the need for any analog frequency shifter. Similarly, in application to the 120-channel transmultiplexer, *K* is chosen to be 72, so that 60 baseband channels are multiplexed in the 312-552 kHz standard basic supergroup band. The total number of samples to be processed in one-way processing, either TDM-to-FDM or FDM-to-TDM, therefore becomes 224 000 (=8000 X 14 X 2) and 1 152 000 (=8000 X 72 X 2) samples per second for the 24- and 120-channel transmultiplexers, respectively. Internal signal processing accuracy is determined to be 20 bits for the 24-channel transmultiplexer and 21 bits for the 120-channel transmultiplexer. The basic clock rate thus becomes 4.48 Mbits/s (=224 kHz X 20) and 24.192 Mbits/s (=1.152 MHz X 21) for 24-channel



(a)



(b)

Fig. 3. Variable delay unit (VDU). (a) Block diagram. (b) Chip photomicrograph.

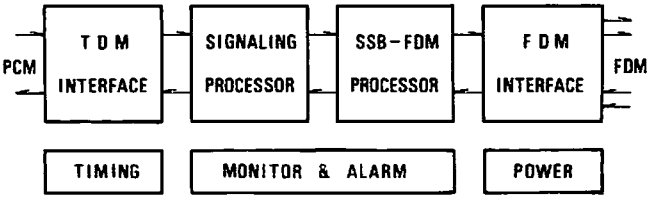
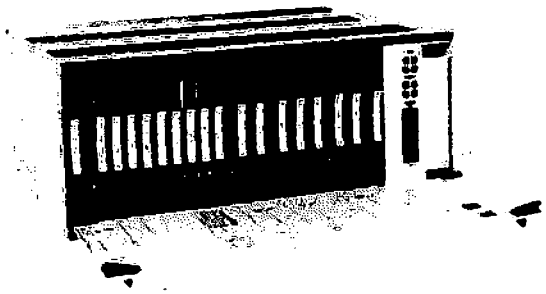
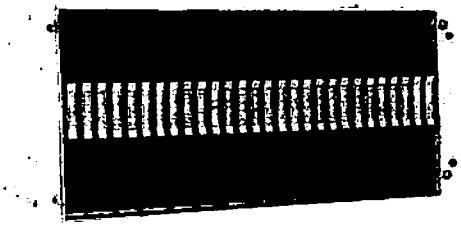


Fig. 4. Digital transmultiplexer functional block diagram.



(a)



(b)

Fig. 5. Equipment external view. (a) 24-channel transmultiplexer. (b) 120-channel transmultiplexer digital portion.

and 120-channel transmultiplexers, respectively. However, the actual clock rate for 120-channel transmultiplexers has been reduced to 1/6 of the basic rate, i.e., 4.032 Mbits/s, by employing a parallelism in hardware implementation.

B. Signaling Processor

Besides the TDM-FDM conversion for voice signals, signaling conversion between PCM and FDM signaling schemes must also be performed within a transmultiplexer. To this end, two modules are provided: 1) out-of-band signaling module and 2) in-band SF signaling module. The out-of-band signaling module maps PCM signaling information to a 3825 (or 3850) Hz tone and vice versa. The in-band SF signaling module performs mutual conversion between PCM signaling and 2600 Hz SF signaling. The module is an all-digital/time division multiplex version of conventional per-channel analog SF signaling adaptors.

C. TDM Interface and Timing

The TDM interface module includes frame buffer memories for bit rate/frame format conversion, code converters between nonlinear PCM codes and linear codes for internal digital signal processing, and signaling bit insertion/extraction to/from the connected PCM stream(s).

The timing module generates the clock signal for internal signal processing by phase locking to one of three sources: 1) an incoming PCM stream, 2) an internal oscillator, and 3) an external reference input. An appropriate source is selected so that both requirements for bit synchronization with the PCM system and for SSB-FDM processing carrier stability are satisfied. When the transmultiplexer is interconnected with a digital switch, the clock is slaved to the incoming signal. When operating with the standard PCM channel bank(s), the highly stable internal oscillator can provide timing information to both internal processors and the PCM channel bank(s). The frame buffer memories in the TDM interface module also have a provision for controlled signal frame slips to allow plesiochronous operation between the incoming PCM signal and the internal signal processing.

D. FDM Interface

The essential elements in this module are A/D and D/A converters and analog bandpass filters. Differing from digital signal processors, whose performance is precisely predictable and stable, performance differences among products and performance degradation with regard to time variation and circumstance condition change are less predictable and less controllable in analog parts. Hence, most of the specification implementation margin is allotted to this module. Adding 1 bit margin to the minimum requirement, according to the calculation based on the method described in [13], the number of bits allotted to A/D and D/A converters is determined to be 14 for the 24-channel transmultiplexer and 13 for the 120-channel transmultiplexer. Table II summarizes the A/D and D/A design parameters.

E. Monitor and Alarm

The entire equipment operation is monitored so that any system failure can be automatically detected and an alarm activated. In addition to conventional monitor alarms, such as power failure, loss of incoming signal, misframe, loss of pilot signals, and reception of remote alarm messages, a series of signal processings, such as law conversions, digital filtering, FFT processing, and A/D and D/A conversions, are monitored for each group or supergroup band and for each direction by using idle time/frequency slots. Frame buffer memory operation is also monitored separately.

V. DIGITAL PROCESSOR DESIGN

A. FFT Processor

The FFT processor function in the multiplexer (TDM-to-FDM direction) is to calculate (1a) and the processor function in the demultiplexer (FDM-to-TDM direction) is to calculate (2a).

1) *14-Point FFT Processor:* Denoting $A_i(Z^K)$ and $\tilde{X}_k(Z^K)$ in (1b) simply as A_i and X_k, respectively, the 14-point FFT processor equation becomes

$$A_i = \sum_{k=0}^{13} X_k \cdot \exp\left\{ j2\pi \frac{4k+1}{56} i \right\}, \quad 0 \leqslant i \leqslant 13. \tag{5}$$

Since sequence $\{X_k\}$; $(k = 0, 1, \cdots, 13)$ is real, sequence $\{A_i\}$; $(i = 0, 1, \cdots, 13)$ has a conjugate symmetry property, such that

$$A_{14-i} = j \cdot A_i^*, \qquad 1 \leqslant i \leqslant 13 \tag{6}$$

where $\{\cdot\}^*$ denotes the complex conjugate of $\{\cdot\}$. With new notations a_i and $\bar{a}_i$ for the real and the imaginary part of A_i,

TABLE II
A/D AND D/A DESIGN PARAMETERS

	Group	Supergroup
Average signal power	3.3 dBm0	6.1 dBm0
Sinusoidal overload point	21.0 dBm0	22.8 dBm0
Sample rate	112 kHz	576 kHz
Number of bits	14 bits	13 bits
Theoretical quantization noise	9.8 pW0p	11.5 pW0p
Implementation margin (A/D + D/A)	9.6 dB	10.6 dB

respectively, the above equation implies that

$$\bar{a}_i = a_{14-i}, \qquad 1 \leqslant i \leqslant 13. \tag{7}$$

Hence, it is only necessary to calculate either the real part or the imaginary part of sequence $\{A_i\}$; $(i = 0, 1, \cdots, 13)$.

Thus, instead of (5), the following DCT equation can be used to derive the desired sequence $\{A_i\}$; $(i = 0, 1, \cdots, 13)$:

$$a_i = \sum_{k=0}^{13} X_k \cdot \cos 2\pi \frac{4k+1}{56} i, \quad 0 \leqslant i \leqslant 13. \tag{8}$$

Next applying a decimation technique developed for FFT algorithms, (8) can be written as

$$a_i = \sum_{k=0}^{6} (X_k + X_{k+7} \cos \pi i) \cos 2\pi \frac{4k+1}{56} i, \qquad 0 \leqslant i \leqslant 13 \tag{9}$$

or

$$a_{2i} = \sum_{k=0}^{6} (X_k + X_{k+7}) \cdot \cos 2\pi \frac{4k+1}{56} 2i, \quad 0 \leqslant i \leqslant 6 \tag{10a}$$

$$a_{2i+1} = \sum_{k=0}^{6} (X_k - X_{k+7}) \cos 2\pi \frac{4k+1}{56} (2i+1), \qquad 0 \leqslant i \leqslant 6. \tag{10b}$$

The above equations indicate that the sequence $\{a_i\}$; $(i = 0, 1, \cdots, 13)$ is gained in two stage processings: first by performing a 2-point DCT $(X_k \pm X_{k+7})$ and then by performing a 7-point DCT.

Fig. 6 illustrates how the above processes are implemented in actual hardware. The implemented processor consists of four subunits: a "2-point DCT calculator," a "data format converter," a "7-point DCT calculator," and a "complex signal former." The 2-point DCT calculator receives the input sequence $\{X_k\}$; $(k = 0, 1, \cdots, 13)$ and calculates $(X_k + X_{k+7})$ and $(X_k - X_{k+7})$ for all values of k from 0 to 6. The resulting sequence (②) is then fed to the data format converter, where serial sequence ② is made parallel in terms of k, and then repeated seven times, thereby forming a new sequence ③. The converter is implemented using VDU chips. New sequence ③ is then fed to the 7-point DCT calculator to generate the

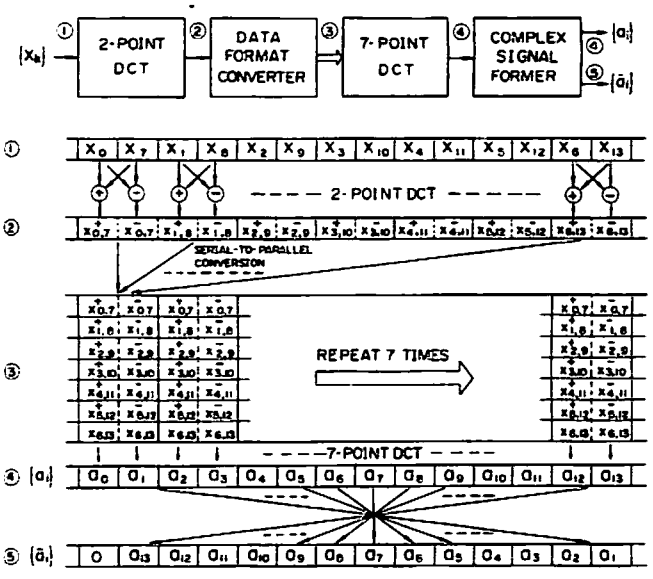


Fig. 6. 14-point FFT processor implementaion.

sequence $\{a_i\}$; $(i = 0, 1, \cdots, 13)$. This calculator can be realized by a direct application of APU function $F2$ listed in Table I. Finally, the complex signal former generates the sequence $\{\bar{a}_i\}$; $(i = 0, 1, \cdots, 13)$ by mapping from $\{a_i\}$; $(i = 0, 1, \cdots, 13)$, according to (7). The entire processor operates at a 4.48 Mbit/s clock rate to process two independent sets of 14-point signals in time division.

Similarly, in the demultiplexer (FDM-to-TDM direction), simple mathematical manipulations, exploiting a property that only real output is needed, derive the following DCT expression in place of (2a):

$$X_k = \sum_{i=0}^{13} c_i \cdot \cos 2\pi \frac{4k+1}{56} i, \qquad 0 \leqslant k \leqslant 13 \tag{11}$$

where $\{c_i\}$; $(i = 0, 1, \cdots, 13)$ is a real sequence derived from complex sequence $\{B_i(Z^{14})\}$; $(i = 0, 1, \cdots, 13)$ by the following relation:

$$c_i = 2(b_i - \bar{b}_{14-i}), \qquad 0 \leqslant i \leqslant 13 \tag{12}$$

where $\{b_i\}$; $(i = 0, 1, \cdots, 13)$ and $\{\bar{b}_i\}$; $(i = 0, 1, \cdots, 13)$ are real and imaginary parts of complex sequence $\{B_i(Z^{14})\}$; $(i = 0, 1, \cdots, 13)$, respectively, and $\bar{b}_{14}$ is defined to be

$$\bar{b}_{14} = \bar{b}_0 = 0.$$

Applying a decimination technique to (11), the following expressions are derived:

$$X_k = \sum_{i=0}^{6} c_{2i} \cdot \cos 2\pi \frac{4k+1}{56} 2i + \sum_{i=0}^{6} c_{2i+1} \cdot \cos 2\pi \frac{4k+1}{56} (2i+1) = P_k + Q_k, \qquad 0 \leqslant k \leqslant 6 \tag{13a}$$

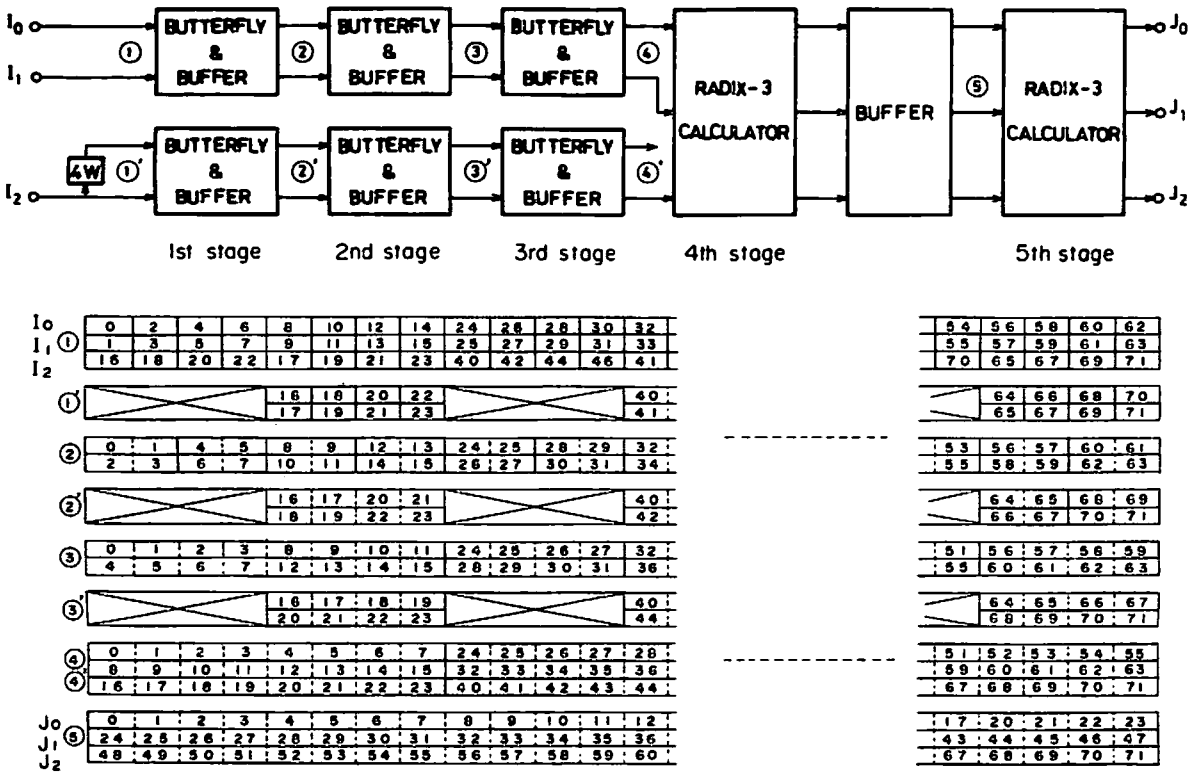


Fig. 7. 72-point FFT processor implementation.

$$X_{k+7} = \sum_{i=0}^{6} c_{2i} \cdot \cos 2\pi \frac{4k+1}{56} 2i - \sum_{i=0}^{6} c_{2i+1} \cdot \cos 2\pi \frac{4k+1}{56}(2i+1)$$

$$= P_k - Q_k, \qquad 0 \leqslant k \leqslant 6 \tag{13b}$$

where

$$P_k = \sum_{i=0}^{6} c_{2i} \cdot \cos 2\pi \frac{4k+1}{56} 2i, \qquad 0 \leqslant k \leqslant 6 \tag{14a}$$

$$Q_k = \sum_{i=0}^{6} c_{2i+1} \cdot \cos 2\pi \frac{4k+1}{56}(2i+1), \qquad 0 \leqslant k \leqslant 6. \tag{14b}$$

Thus, the processor is implemented by a series of a "real signal former," a "data format converter," a "7-point DCT calculator," and a "2-point DCT calculator." The real signal former receives complex sequence $\{B_i\}$; $(i = 0, 1, \cdots, 13)$ and converts it into real sequence $\{c_i\}$; $(i = 0, 1, \cdots, 13)$ according to (12). The real sequence is then fed to the data format converter followed by the 7-point DCT calculator. In the 7-point DCT calculator, (14a) and (14b) are calculated in even and odd timeslots, respectively. The 2-point DCT calculator finally calculates (13a) and (13b).

2) *72-Point FFT Processor:* Following the 120-channel transmultiplexer design previously reported [13], the 72-point FFT processor has been realized by three radix-2 stages and two radix-3 stages in tandem. However, use of LSI's with different architecture and different operation speed has resulted in a different processor structure.

Fig. 7 shows a block diagram and relevant sequence charts for the FFT processor used in both the multiplexer and the demultiplexer. 72 incoming samples are carried by three complex signal lines (I_0-I_2), each carrying 24 samples within a frame according to the order shown in the sequence charts.

Since a radix-2 butterfly arithmetic module can accept only two complex input signals, two parallel sets of three radix-2 stages are provided. The first two signals (I_0, I_1) are fed to the upper three radix-2 stages. The remaining one signal (I_2) is split into two signals, as shown in sequence chart ①′, and then supplied to the lower three radix-2 stages. Hence, the lower three radix-2 stages are only busy for half the frame duration.

Each radix-2 stage consists of an APU chip, performing function *F5* (butterfly arithmetic calculator), and a VDU chip, serving as a sample sequence interchange memory. Using one-word delay ($1W$), two-word delay ($2W$), and four-word delay ($4W$) in the first stage, the second stage, and the third stage, respectively, the order of samples is interchanged as ①→②→③→④ and ①′→②′→③′→④′ in sequence charts.

Three complex signals, two from the upper third stage (④) and one from the lower third stage (④′), are then supplied to the fourth stage where three 3-point DFT calculations are to be performed. Since an APU chip can calculate one 3-point DFT by function *F4* listed in Table I, use of three APU chips is sufficient to complete the required function. The fifth stage has the same configuration, and performs three 3-point DFT calculations on signals ⑤ that are derived from an interstage buffer after the fourth stage calculator.

Except for three dual 4-1 data selector IC's used in the

interstage buffer between the fourth and fifth stages, all functional elements in Fig. 7 are made up of DSP chips.

B. Digital Filter

As described in Section II, the SSB-FDM processor utilizes digital filters with purely real and imaginary coefficients. Such a complex coefficient filter can be implemented using an APU chip and a VDU chip, as shown in Fig. 8. The hardware amount needed to implement such a complex coefficient filter is only twice that required for ordinary real coefficient filter implementation.

The upper half portion and the lower half portion are assigned to the real signal path and the imaginary path, respectively. Cross connections between both signal paths correspond to the purely imaginary coefficients. The amount of delay (M) in the delay elements for the first-order coefficients is 50 bits less than the amount of delay (N) in the delay elements for the second-order coefficients, to compensate for the processing delay in multipliers, adders, and overflow correctors. Since the maximum length of a delay unit in a VDU chip is 519 bits, the maximum number of channels processed in time division by the circuit shown in Fig. 8 is equal to the integer part of $(519/B)$, where B is the sample wordlength. The overflow correctors (OFC) prevent any large amplitude limit cycle oscillation. The built-in scalers (S) are used for scaling the input signals. Filter coefficients and scaling coefficients are supplied from outside the chip through coefficient input terminals. Two coefficients, differing only in sign, can be supplied from a single source, since the coefficient polarity can be inverted within an APU chip.

In order to determine filter coefficients, transfer function $G(Z)$ needs to be designed. Since $G(Z)$ must then be broken down to $\{G_i(Z^K)\}$; $(i=0,1,\cdots,K-1)$ as described in Section II, it is convenient to design $G(Z)$ so that its denominator polynomial is only a function of Z^K. A simple approach to achieve this is to design $G(Z)$ as a cascade of a channel shaping recursive filter at 8 kHz sample rate and a multistopband nonrecursive filter at $8 \times K$ kHz rate [6], [13]. However, progress in computer-aided filter design techniques [23] has made it possible to design $G(Z)$ directly as a single multirate filter with numerator polynomial $N(Z)$ and denominator polynomial $D(Z^K)$. Actual designs have indicated that $D(Z^K)$ becomes eighth-order for both $K = 14$ and $K = 72$, and that the number of taps in $N(Z)$ becomes 112 for $K = 14$ and 576 for $K = 72$, respectively. Thus, in either $K = 14$ or $K = 72$, $G(Z)$ breaks into a set of eighth-order 8 kHz rate filters with Z-transfer functions $\{G_i(Z^K)=N_i(Z^K)/D(Z^K)\}$; $(i = 0, 1, \cdots, K-1)$. The resulting 8 kHz rate filters are configured in a cascade of four biquad sections with purely real and imaginary coefficients of 14 bit accuracy. Hardware implementation is thus achieved by just connecting four biquad filters of the structure shown in Fig. 8, although implementation for $K = 72$ requires three hardware units provided in parallel. Since a sync pulse needed to indicate the LSB location in data words, supplied to each section, is relayed through sections, no IC chips other than the DSP chips are required to realize a higher order filter, irrespective of the data wordlength.

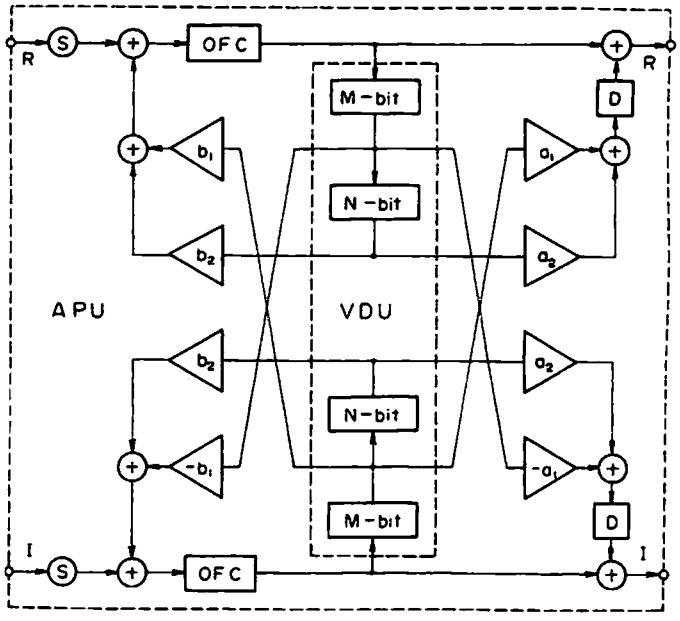


Fig. 8. Complex biquad filter section realized by an APU chip and a VDU chip.

Fig. 9 shows, as an example, an overall frequency response calculated for a cascade of the 14-point FFT processor and a set of eighth-order complex coefficient digital filters used in the 24-channel transmultiplexer. All coefficients used in the FFT processor and digital filters are truncated to 14 bits. Differing from using a cascaded connection of a slow recursive filter and a fast nonrecursive filter, the frequency response does not show an excessive loss at every other 4 kHz band in the out-of-band region.

VI. PERFORMANCE

Both 24- and 120-channel transmultiplexers have satisfied all the performance requirements specified in CCITT Recommendation G.792 with considerable margins.

Fig. 10 shows in-band transmission characteristics for the complete chain from the FDM signal input port to the FDM signal output port with digital ports loopback. The absolute delay was measured as no more than 2.5 ms in the 24-channel transmultiplexer and no more than 2.0 ms in the 120-channel transmultiplexer. This difference is mainly due to the characteristics of the analog bandpass filters employed.

Fig. 11 indicates that both transmultiplexers have a very good gain tracking performance within the whole input signal range. This is an evidence for the merits of high precision digital signal processing.

Signal-to-total distortion ratio was measured as a function of the input signal level by connecting a channel translator and a group translator (only for the 120-channel transmultiplexer measurement) in tandem with the transmultiplexer, looped back at the digital ports. The results are very satisfactory, as shown in Fig. 12, in spite of FDM terminal noise inclusion.

Intelligible crosstalk was better than 67 dB in both the 24- and 120-channel transmultiplexers. The worst idle channel noise was −71 dBm0p and −70.5 dBm0p in the 24- and the 120-channel transmultiplexer, respectively.

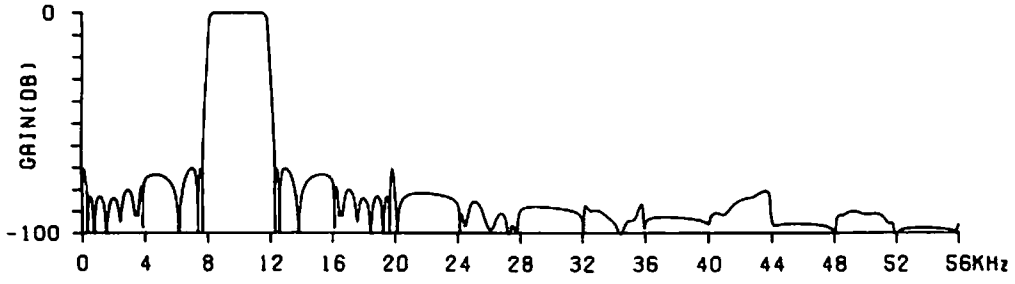
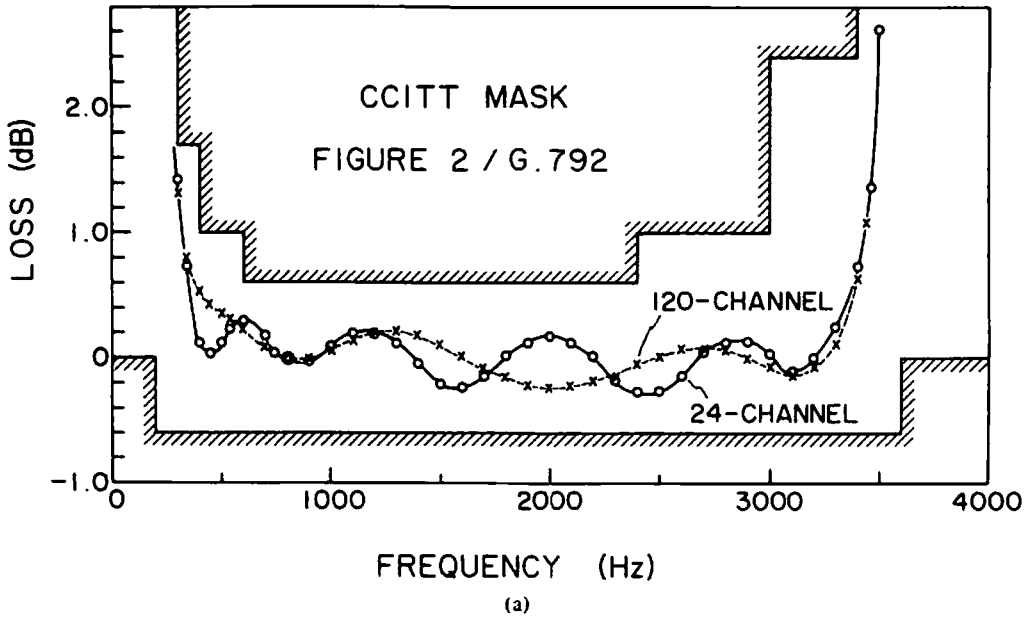
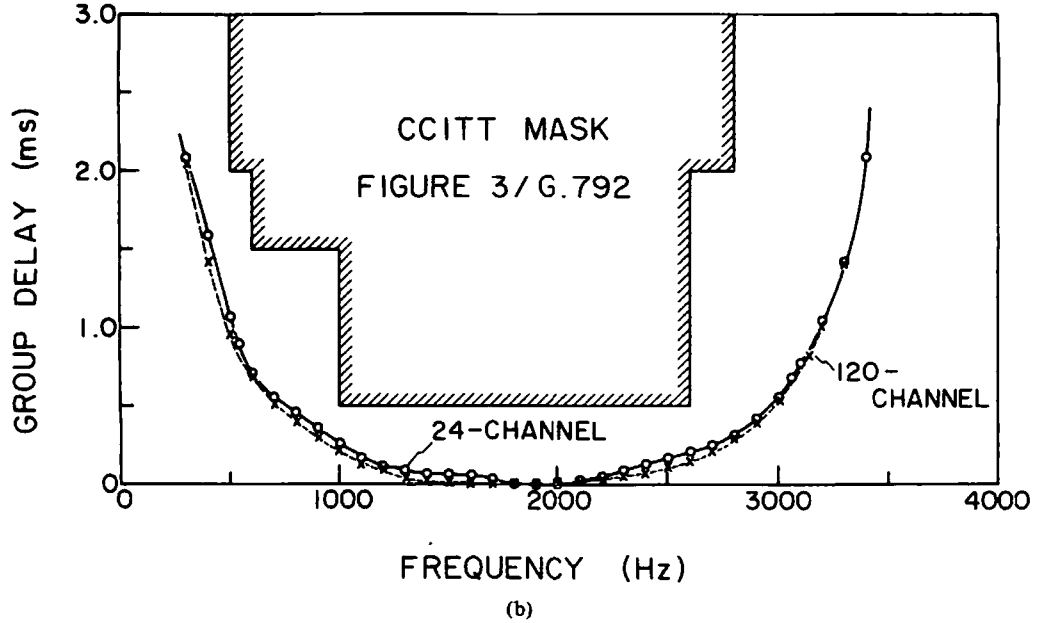


Fig. 9. Calculated overall frequency response for the SSB-FDM processor in the 24-channel transmultiplexer.



(a)



(b)

Fig. 10. In-band transmission characteristics. (a) Amplitude loss. (b) Group delay distortion.

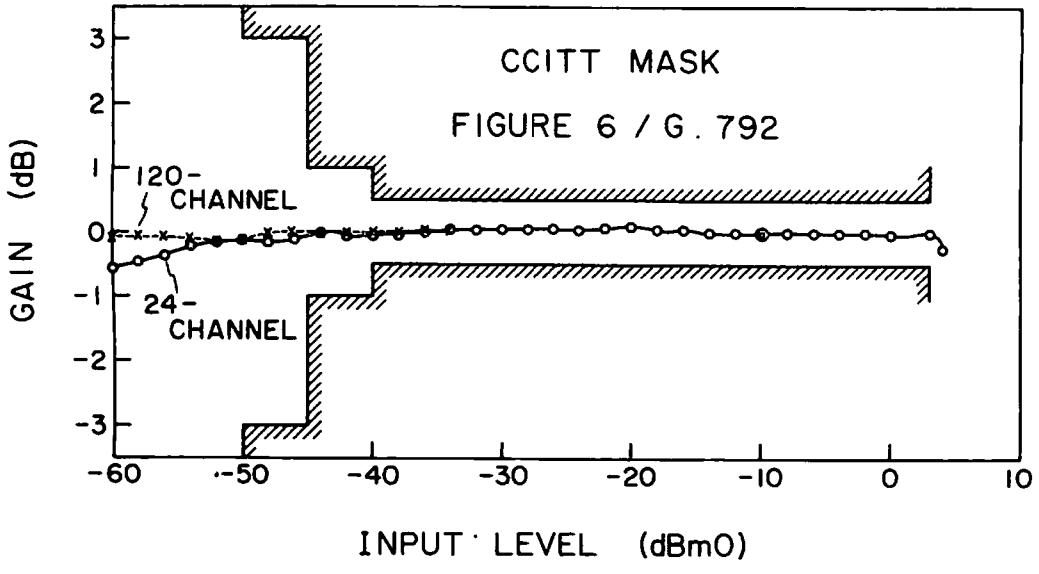


Fig. 11. Gain variation with a function of input signal level.

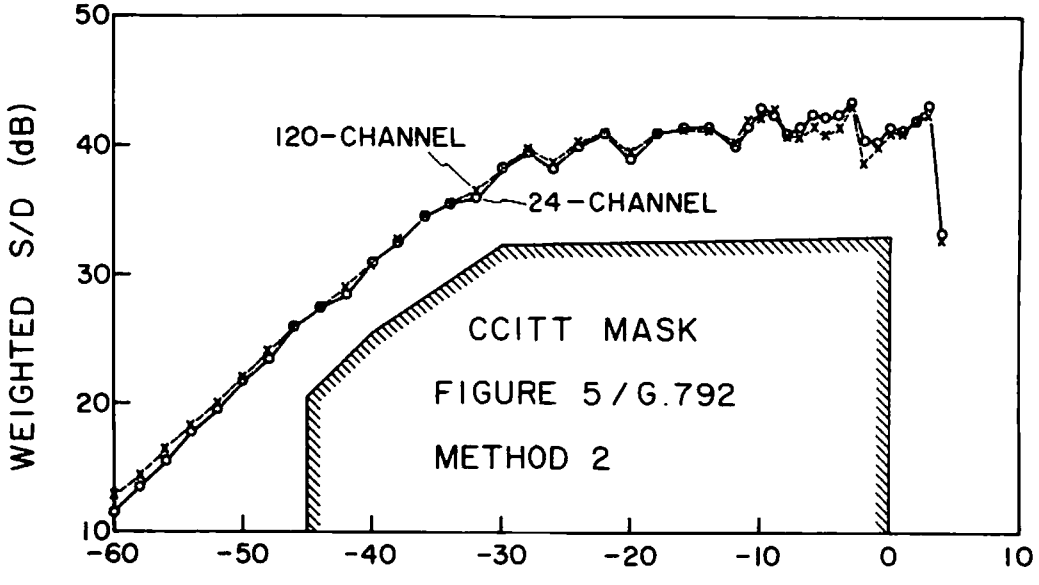


Fig. 12. Signal-to-total distortion ratio performance measured in a VF channel.

Fig. 13(a) and (b) shows group band and supergroup band noise loading *S/D* performance. Curves designated as "CODEC LOOPBACK" indicate the performance for an FDM codec only, and those labeled as "TDM LOOPBACK" show the performance for the entire transmultiplexer looped back at the digital ports. Thus, the difference between these curves is due to digital signal processing. The difference between two curves in Fig. 13(a) is almost constant, up to a larger input signal level. However, the difference in Fig. 13(b) becomes larger as the signal level increases from a point around 0 dBm0, showing a crosstalk contribution. If digital filter stopband attenuation is finite, signal power from all other loaded channels crosstalks to any particular channel through decimation and interpolation processes. The *S/D* value due to the crosstalk power is constant, regardless of the signal power. Hence, the effect is visible only at a larger signal level in Fig. 13(b). The effect is not visible in Fig. 13(a), because of the small number of channels and higher average stopband attenuation in the employed filter.

VII. CONCLUSION

Two new digital transmultiplexers, a 24-channel transmultiplexer and a 120-channel transmultiplexer, have been developed to provide an efficient means for interconnecting emerging digital communication systems and existing analog facilities. The use of the newly developed high-level DSP LSI chips has reduced not only the equipment size, power, and cost, but has drastically reduced the load for the equipment design, fabrication, and test. Although not expected *a priori*, the extensive use of the new LSI chips has also led to a re-

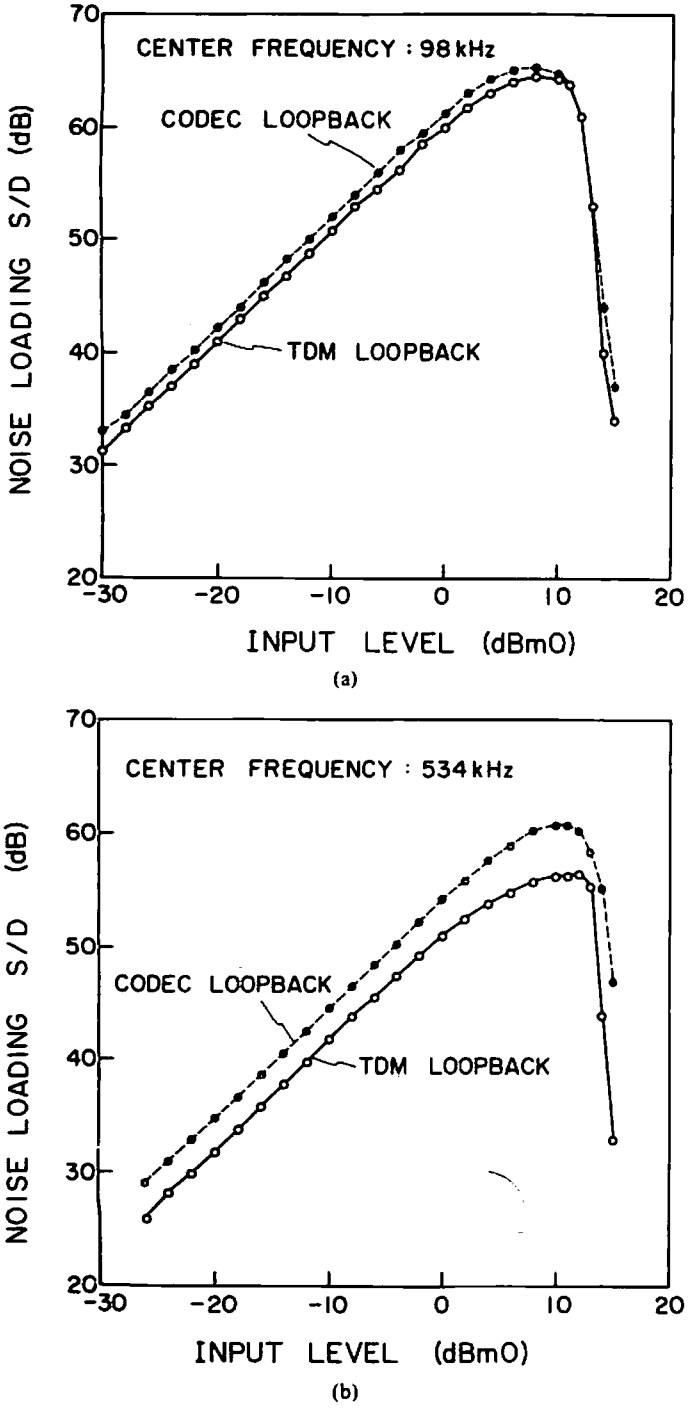


Fig. 13. Signal-to-total distortion ratio performance measured in the FDM band using noise loading method. (a) 24-channel transmultiplexer. (b) 120-channel transmultiplexer.

duction in the noise level around the digital processor, minimizing interferences to A/D and D/A operations. The measured performance has satisfied all the requirements specified in CCITT Recommendation G.792 with considerable margins.

ACKNOWLEDGMENT

The authors wish to acknowledge the technical contribution of N. Kawayachi, Y. Morimura, Y. Nakanishi, and Y. Shimada on hardware design and evaluation works. The authors are also indebted to Dr. H. Kaneko, Y. Kato, A. Tomozawa, Dr. A. Sawai, Y. Katagiri, and S. Tanaka for their encouragement and managerial efforts throughout the project, and to Y. Ishizaki, N. Yoshida, and Y. Sakamura for efforts on the LSI development.

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