A Single-Chip 20-Channel Speech Spectrum Analyzer Using a Multiplexed Switched-Capacitor Filter Bank

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Abstract—A single-chip speech spectrum analyzer which contains a 20-channel filter bank, a 9 bit resolution analog-to-digital converter, and a 396 bit buffer memory is described. Several efficient design techniques were used to realize the equivalent 308th-order transfer functions on a single chip monolithic MOS circuit. A new time division multiplexed switched-capacitor filter technique is introduced which can easily cancel dc offsets which appear in the multiplexed channel outputs. The LSI was fabricated in 3.5 μm CMOS technology, with a 7.0×6.5 mm^2 die size and a 150 mW power consumption with a +5 V single power supply. Experimental results show that designed performance was realized.

I. Introduction

AUTOMATIC speech recognition has become an important technique for man–machine interface in various application fields [1]. Advanced LSI technology has promoted the developments of economical and compact speech recognition systems. Recently, several speech recognition LSI's have been developed. For example, a single-chip LSI and LSI chip sets [2]–[5] have been reported. These are, however, mainly directed toward miniaturizing the speech recognition systems and are not suited to achieving high-level recognition performances for various categories of spoken words to be recognized. For example, a Japanese monosyllable recognition system, having a 20-channel filter bank, is still built on multiple mounting boards [6].

This paper presents a single-chip high-level speech spectrum analyzer fabricated using 3.5 μm CMOS technology [7], [8].

There exist a number of speech analysis methods, including the bandpass filter bank, FFT, linear predictive coefficients (LPC), LPC cepstrum, and PACOR coefficient techniques [9]. From among them, we choose the classical filter bank approach for the following reasons. First, it can provide stable analysis performance for speech recognition. Second, the many filters required in a filter bank can be effectively realized in a small area, with low power dissipation, by using analog MOS technology.

In order to achieve precise spectrum resolution, a 20-channel filter bank is employed. Each channel consists of a 6th-order bandpass filter, a rectifier, and an 8th-order low-pass filter. Furthermore, to obviate the necessity for external circuits and to realize a flexible analog-to-digital (A/D) interface with CPU, an A/D converter and a buffer memory are also included.

Several useful design techniques, particularly for switched-capacitor filters and noise suppression in analog circuits, are introduced in order to implement the above high-level functional blocks in a single-chip monolithic MOS circuit.

II. Spectrum Analyzer System Description

Fig. 1 shows a functional block diagram for a speech spectrum analyzer to be implemented on a single chip MOS circuit.

An automatic gain controller (AGC) is under the CPU control and adjusts the input signal level over 46.5 dB dynamic range in 1.5 dB steps. A prefilter is synthesized by combining a 2nd-order RC active filter and a 10th-order switched-capacitor filter (SCF). It is used for antialiasing and sampling frequency reduction from 200 kHz to 18.18 kHz. A 1st-order SC equalizer (EQL) has about 6 dB/oct amplitude response, and is used for emphasizing the high-frequency spectrum. A bandpass filter (BPF) bank contains 22-channel BPF's synthesized with 6th-order SCF's. Their calculated amplitude responses are listed in Table I. Twenty channels are used for spectrum analysis. The remaining two channels are prepared to observe dc offsets. The BPF bank outputs are full wave rectified. Spectra corresponding to the BPF center frequencies are extracted through a 22-channel low-pass filter (LPF) bank. The LPF for each channel is synthesized by an 8th-order SCF. The LPF cutoff frequencies determine the integration interval for the rectifier outputs, which must be optimized according to speech spectrum transition behavior. For this pur-

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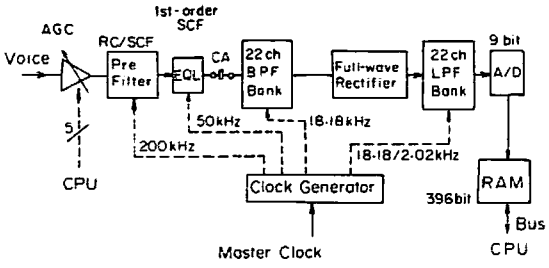

Fig. 1. Speech spectrum analyzer LSI block diagram.

TABLE I
CALCULATED BPF AMPLITUDE RESPONSES

Channel Number	Center Frequency (Hz)	−3dB Bandwidth (Hz)
1	485	270
2	730	280
3	980	280
4	1220	260
⋮	⋮	⋮
15	3900	280
16	4145	290
17	4520	540
18	5005	510
19	5735	990
20	6700	1000
21	Dummy	—
22	Dummy	—

pose, the LPF's have programmable cutoff frequencies which can be selected from 12.5, 25, 50, 100, 200, and 400 Hz frequencies through the CPU control. An A/D converter, which is implemented with a capacitor array, has 9 bit resolution. The converted digital speech spectra are stored in a double buffer memory with 396 bit capacity and can be asynchronously read out by the CPU.

Since the A/D converter is shared by 22-channal signals during a 1 ms minimum frame period, the conversion time for each channel signal becomes 45 μs.

Both the BPF and LPF banks contain 308th-order filters as a whole. Therefore, in order to successfully realize such very high-order filters, together with the 9 bit resolution A/D converter and the 396 bit memory on a single-chip monolithic MOS circuit, switched-capacitor filter techniques are inherently required, and significant reductions in their occupied area and power dissipation must be accomplished. In the next section, several design techniques for SCF's, which are directed toward the above goal, are introduced.

III. SWITCHED-CAPACITOR FILTER DESIGN

A. Transfer Function Approximation

Transfer functions for the BPF's are approximated so as to have Gaussian amplitude responses in the passband and stopband attenuation of more than 40 dB through an iterative approximation method. The LPF's integrate the spectra during the specified time interval. Their impulse response, therefore, becomes a weighting function for the

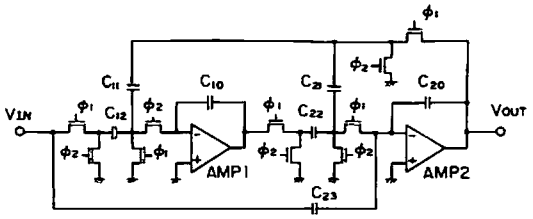

Fig. 2. Biquad section for state variable SCF.

rectifier outputs, and is required to have a symmetrical form. For this purpose, poles of the transfer function are determined from the Bessel polynomial, and zeros, located on the unit circle are optimized so as to realize equiripple stopband attenuation of more than 50 dB.

B. Sampling Frequency Alternation

In order to simplify an RC active filter, which usually occupies a large chip area, the input continuous speech signal is first sampled with a high sampling frequency of 200 kHz. After suppressing high-frequency components by an SC filter, the sampling frequency is reduced from 200 to 18.18 kHz allowing for compression of the capacitor ratio ranges in both BPF's and LPF's. Furthermore, the LPF is realized as a cascade form of two 4th-order LPF's. They operate with 18.18 and 2.02 kHz sampling frequencies, and have high and low cutoff frequencies, respectively. The 4th-order LPF with high sampling frequency serves as an antialiasing filter for the sampling frequency change from 18.18 to 2.02 kHz.

C. SCF Circuit Configuration

The SCF's are synthesized as a cascade form of state variable biquad sections shown in Fig. 2. The transfer function is given by

$$H(z)=\frac{\alpha_{23}+(\alpha_{12}\alpha_{22}-2\alpha_{23})z^{-1}+\alpha_{23}z^{-2}}{1+\alpha_{21}+(\alpha_{11}\alpha_{22}-2-\alpha_{21})z^{-1}+z^{-2}} \quad (1a)$$

$$\alpha_{1i}=C_{1i}/C_{10},\ \alpha_{2i}=C_{2i}/C_{20}. \quad (1b)$$

D. Capacitor Value Scaling

Although the sampling frequencies are optimized, the ratios of the sampling frequencies to the bandwidths are still large in some cases because the frequency range to be covered is wide. Further compression of the capacitor ratio ranges is achieved through scaling up small value capacitors by dividing their voltage. Two kinds of voltage divider circuits, including capacitive and resistive dividers, exist [10], [11]. As will be described in the next section, the filter banks are synthesized by time division multiplexed SCF techniques. In such a case, the capacitive divider is not desirable because one capacitive divider cannot be shared by the multiplexed channels, as when capacitor C_{23} needs to be scaled up. On the other hand, a resistive divider does not hold any charge and can be shared by all channels. For

this reason, a resistive divider is employed for scaling up the value of capacitor C_{23} in the BPF's, and the values of C_{11}, C_{21}, and C_{23} in the LPF's. When the smallest capacitor value is normalized as unity, 40 percent of the total capacitance can be saved through the above capacitor value scaling.

E. Discrete Value Capacitor Optimization

In addition to compressing the ranges of capacitor ratios, it is necessary to reduce the amount of capacitance required.

As is well known, SCF performances are determined by the capacitor ratios. Therefore, the above requirement can be rephrased as to obtain high capacitor ratio accuracy using small value capacitors. For this purpose, all capacitors are synthesized using a plural number of the same unit capacitors having the same dimension. Although capacitor value deviations caused by edging errors are relatively large, their effects on the capacitor ratios are small. Therefore, a very small unit capacitor can be used. In this case, the capacitors equivalently have integer values, and therefore, their values must be discretely optimized.

An efficient discrete optimization technique [12], which has been developed for SCF's, is employed for this purpose. In this method, first, the capacitor values are modified so as to decrease roundoff errors. Second, effective capacitors are selected taking their sensitivity into account. Optimum discrete values for these capacitors are searched for around the initial values obtained by rounding off the modified capacitor values. The maximum amplitude response deviation is used for an error criterion.

IV. Time Division Multiplexed SCF's

A most important technique to develop a single-chip LSI, including the very high-order filters mentioned previously, is to synthesize the filter banks using time division multiplexed (TDM) SCF's. In TDM SCF's, an operational amplifier (op amp) and several of the capacitors can be shared by multiplexed channels.

A. Existing TDM SCF's

First, the existing TDM SCF's are briefly described here [13]. SCF's are sampled-data filters. In other words, charges representing internal signals are transferred by switching and are stored in capacitors during a sampling period. Therefore, by increasing a clock frequency, it is possible to share a single SCF among multichannels. In the SC biquad section shown in Fig. 2, the capacitors C_{10}, C_{20}, and C_{23} always hold charges. Therefore, this kind of capacitor is individually required for mutliplexed channels. On the other hand, the capacitors C_{11}, C_{12}, C_{21}, and C_{22} transfer charges from one integrator to the next, and are discharged in half a clock period. Therefore, these capacitors can be shared by multiplexed channels. The clock frequencies for the TDM SCF's increase from 18.18 to 400 kHz (=18.18 kHz×22 channels) and from 2.02 to 44.44 kHz (= 2.02 kHz×22 channels).

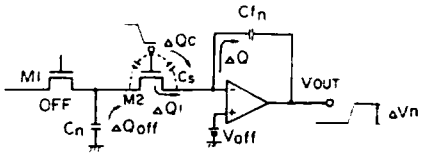

Fig. 3. DC offset source model for SC integrator.

However, certain problems must be overcome in order to successfully apply the TDM SCF's. These problems include high-speed op amp implementation, crosstalk between multiplexed channels through parasitic capacitors in MOS switches, and dc offsets which usually differ from channel to channel. DC offsets seem to be the dominant problem, and are analyzed in detail in the next paragraph.

B. DC Offset Analysis

DC Offset Sources: Fig. 3 shows a model of dc offset sources. Charge leak ΔQ from the integrator capacitor C_{fn} is caused by the op amp input offset $\Delta Q_{off} = C_n V_{off}$, clock feedthrough $\Delta Q_c = C_s V_{DD}$, which leaks through gate overlap capacitors, and channel charge injection $\Delta Q_i = f(C_n, C_{fn})$ being a function of C_n and C_{fn}. Exactly speaking, variables of the ΔQ_i function further include the rise and fall times of the clock waveforms. They have, however, the same value among the multiplexed channels, and are not taken into account. Therefore, ΔQ is expressed by

$$\Delta Q = \Delta Q_{off} + \Delta Q_c + \Delta Q_i \tag{2a}$$

$$= C_n V_{off} + C_s V_{DD} + f(C_n, C_{fn}). \tag{2b}$$

Index n means the channel number. Output offset voltage ΔV_n is determined by

$$\Delta V_n = \Delta Q / C_{fn}. \tag{3}$$

From (2b),

$$\Delta V_n = \left\{ C_n V_{off} + C_s V_{DD} + f(C_n, C_{fn}) \right\} / C_{fn}. \tag{4}$$

Since C_n and C_{fn} usually have different values among the multiplexed channels, the ΔV_n values also become different.

DC Offset Transfer Function: Equation (4) can be equivalently expressed as

$$\Delta V_n = C_n \tilde{V}_{off,n} / C_{fn} \tag{5a}$$

$$\tilde{V}_{off,n} = V_{off} + \frac{C_s}{C_n} V_{DD} + \frac{f(C_n, C_{fn})}{C_n}. \tag{5b}$$

This means the charge leaks ΔQ_c and ΔQ_i are equivalently expressed as op amp input offsets.

Output Offsets of Biquad Section: Letting $T_1(z)$ and $T_2(z)$ be transfer functions from the first and second op amp inputs to the biquad section output shown in Fig. 2, they are

$$T_1(z) = \frac{-\alpha_{22}(\alpha_{11} + \alpha_{12})}{\alpha_{11}\alpha_{22} z^{-1} + (1 - z^{-1})(1 + \alpha_{21} - z^{-1})} \tag{6a}$$

$$T_2(z) = \frac{(1 - z^{-1})(\alpha_{21} + \alpha_{22})}{\alpha_{11}\alpha_{22} z^{-1} + (1 - z^{-1})(1 + \alpha_{21} - z^{-1})}. \tag{6b}$$

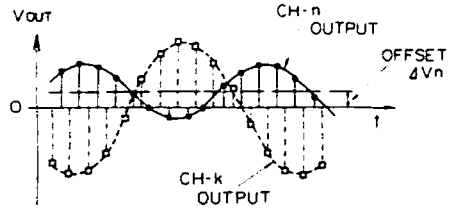

Fig. 4. Output dc offsets in TDM SCF.

By letting $z=1$, transfer gains at the dc frequency can be obtained as follows:

$$T_1(z)|_{z=1} = -\frac{C_{11}+C_{12}}{C_{11}} \tag{7a}$$

$$T_2(z)|_{z=1} = 0. \tag{7b}$$

The output offsets $\Delta V_{\text{out},n}$ for the multiplexed channels are given by

$$\Delta V_{\text{out},n} = -\frac{C_{11,n}+C_{12,n}}{C_{11,n}}\tilde{V}^{(1)}_{\text{off},n} \tag{8}$$

where, $\tilde{V}^{(1)}_{\text{off},n}$ means the equivalent input offset voltage of the first op amp. In (8), the dc transfer gain and offset source magnitude for the multiplexed channels are different from each other; therefore, the output offsets $\Delta V_{\text{out},n}$ also differ. Fig. 4 illustrates multiplexed output offset examples.

C. New TDM SCF's

The idea behind the new TDM SCF's is to make the equivalent op amp input offsets $\tilde{V}_{\text{off},n}$ uniform in their magnitude for all channels. From (4) and (5), uniforming the offset source magnitudes can be carried out through making C_n and C_{fn} uniform in their values. Fig. 5(a) and (b) shows basic structures for conventional and proposed TDM SCF's, respectively. Since C and C_f have the same values for all channels in the new method, $\tilde{V}_{\text{off},n}$, as well as ΔV_n become uniform in their values. Equivalent capacitor ratios are realized by dividing the capacitor voltages with a resistor string. Then new TDM SCF idea can be applied to the biquad section, as shown in Fig. 6.

The transfer functions corresponding to (6) in the new structure are expressed by

$$T_{1R}(z) = \frac{-\tilde{\alpha}_{22}(\alpha_{11}+\alpha_{12})}{\tilde{\alpha}_{11}\tilde{\alpha}_{22}z^{-1}+(1-z^{-1})(1+\tilde{\alpha}_{21}-z^{-1})} \tag{9a}$$

$$T_{2R}(z) = \frac{(1-z^{-1})(\alpha_{21}+\alpha_{22})}{\tilde{\alpha}_{11}\tilde{\alpha}_{22}z^{-1}+(1-z^{-1})(1+\tilde{\alpha}_{21}-z^{-1})} \tag{9b}$$

$$\tilde{\alpha}_{ij} = k_{ij,n}\alpha_{ij} \tag{9c}$$

where, $k_{ij,n}$ is a resistor ratio for the nth-channel, which determines an equivalent capacitor ratio as $k_{ij,n}C_{ij}/C_{io}$. By letting $z=1$ in (9), the dc transfer gains become

$$T_{1R}(z)|_{z=1} = -\frac{C_{11}+C_{12}}{C_{11}k_{11,n}} \tag{10a}$$

$$T_{2R}(z)|_{z=1} = 0. \tag{10b}$$

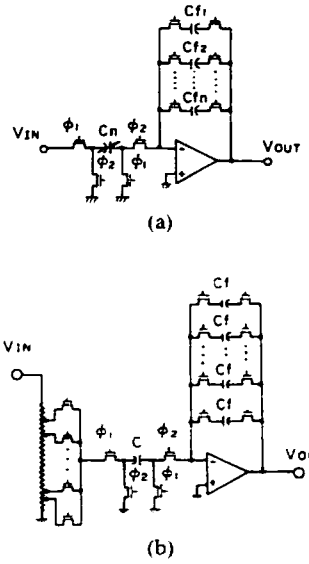

Fig. 5. TDM SC integrator structures. (a) Conventional type. (b) New type.

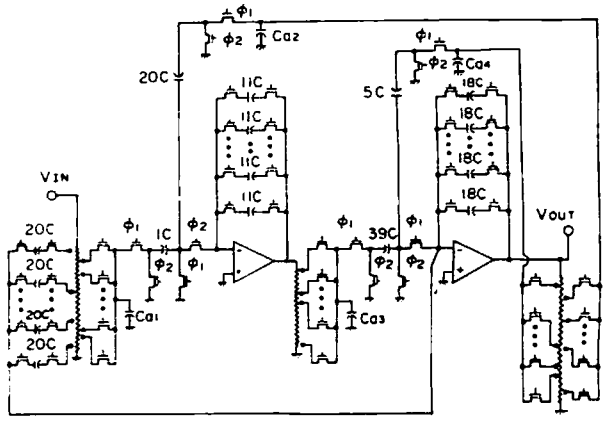

Fig. 6. New TDM SCF biquad with resistor strings.

Furthermore, the output offsets $\Delta V_{\text{out},n}$ can be expressed by

$$\Delta V_{\text{out},n} = -\frac{C_{11}+C_{12}}{C_{11}k_{11,n}}\tilde{V}^{(1)}_{\text{off},n}. \tag{11}$$

Since $\tilde{V}^{(1)}_{\text{off},n}$ and the capacitors C_{11} and C_{12} are uniformed, $\Delta V_{\text{out},n}$ is inversely proportional to $k_{11,n}$. Equation (11) means $\Delta V_{\text{out},n}$ still differ from channel to channel. In this case, however, the offset source magnitudes are uniformed. Hence, $\tilde{V}^{(1)}_{\text{off},n}$ can be cancelled by adding the same voltage to the first op amp input. Consequently, the output offsets for all channels can be suppressed. The same compensatory offset voltage can make it possible to share a single offset cancelling circuit among all multiplexed channels. The compensatory offset voltage can be determined by monitoring the output offset in the dummy channel.

In the BPF case, it is possible to suppress a part of the output offsets transferred from the first and second biquad sections by assigning the 2nd-order transfer function with transmission zeros at the dc frequency point to the last biquad section.

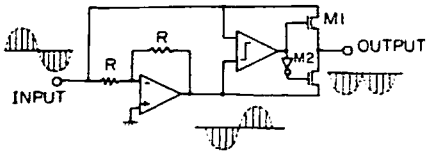

Fig. 7. Full wave rectifier.

Additional capacitors (C_{a1}–C_{a4}) in Fig. 6 are used for reducing variation in the dc offsets, due to source impedance deviations [14].

D. Resistor Ratio Optimization

Equivalent capacitor ratios are determined from both capacitor ratios and resistor ratios. Since the same capacitor values are used for all multiplexed channels in the new TDM SCF's, the actual capacitor ratios must be discretely optimized over all channels. On the other hand, the resistor ratios can be determined so as to individually optimize a filter response for each channel. In order to obtain high precision resistor ratios using small resistors, it is necessary to realize resistors using a plural number of unit resistors. Therefore, the optimum resistor ratios are discretely searched for in the specified regions. Both discrete optimization procedures are simultaneously carried out. The mean-square error of equivalent capacitor ratios is taken as an error criterion. The total number of unit resistors is determined through the above optimization procedure, so as to obtain the desired SCF amplitude responses. Calculated results require 198 unit resistors for each resistor string.

E. Low-pass Filter Bank

The LPF's are designed so as to have the same transfer function for lowband channels (channels 1–11) and highband channels (channels 12–22). Therefore, the output offsets in each group of channels have the same value. The output offsets of the two groups are monitored by the two prepared dummy channels, and are cancelled in the CPU. In this case, therefore, the existing TDM SCF technique can be employed.

V. Other Functional Blocks

A. Rectifier

The circuit shown in Fig. 7 has an inverting path and a noninverting path. A comparator selects one of them according to input polarity. A positive signal passes through the inverting path, and a negative input passes through the noninverting path. As a result, a full-wave rectified output is obtained. Using a high-speed comparator, a fast rectifier shared by 22 channels can be realized.

B. A/D Converter

The A/D converter is synthesized by a charge redistribution technique [15]. A capacitor array consists of 255 unit capacitors and a 1/2 unit capacitor. A 0.3 pF unit capacitor is employed. The conversion time is 45 μs and a full scale voltage range is 1 V.

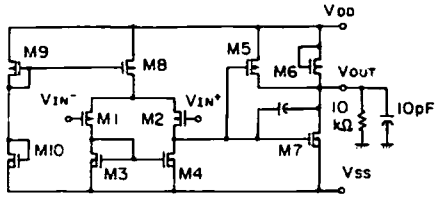

Fig. 8. Operational amplifier schematic.

TABLE II
Operational Amplifier Characteristics

DC gain	71 dB
Unity gain frequency	4.1 MHz
Slew rate	6.5 V/μs
1% settling time (1 V step: 10 pF + 10 kΩ load)	400 ns
Power consumption	5.3 mW
Area	0.05 mm^2

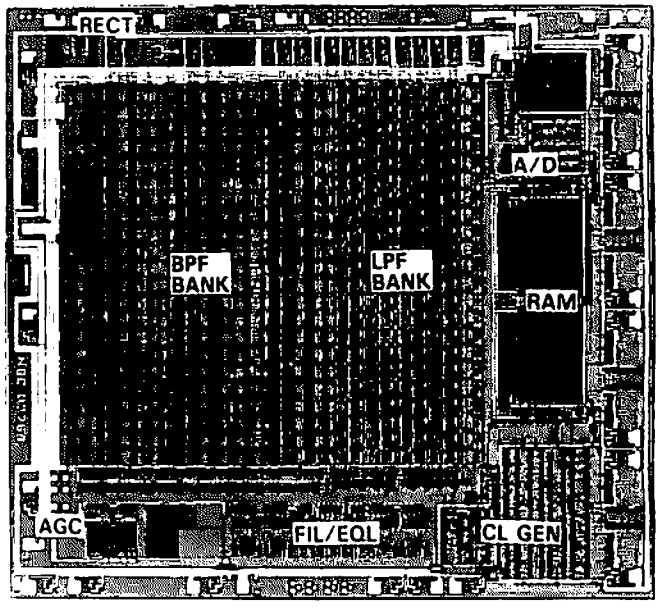

Fig. 9. Chip photomicrograph.

VI. LSI Implementation

A. Operational Amplifier

The multiplexed SCF shown in Fig. 6 requires an operational amplifier which is sufficiently fast to handle 400 kHz sampled signals and has a low-impedance output capable of driving a resistive divider. As shown in Fig. 8, it consists of two stages. The input stage is a differential amplifier with a 45 dB gain. The output stage is a modified CMOS inverter consisting of transistors $M5$, $M6$, and $M7$, with a 26 dB gain.

The output impedance mainly depends on transistor $M5$ source–drain resistance, which operates in triode mode. An additional transistor $M6$ keeps the output impedance low

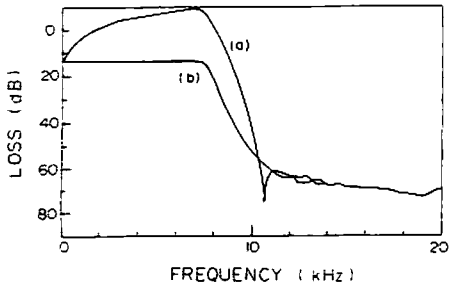

Fig. 10. Amplitude responses in dB for cascade form of SC equalizer and prefilter. (a) With equalizer. (b) Without equalizer.

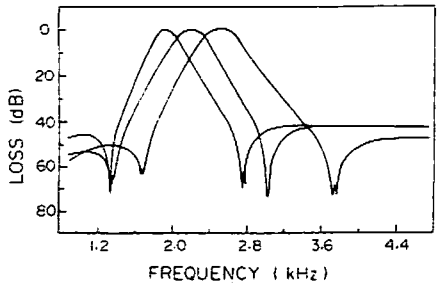

Fig. 11. Examples for 20-channel BPF amplitude responses.

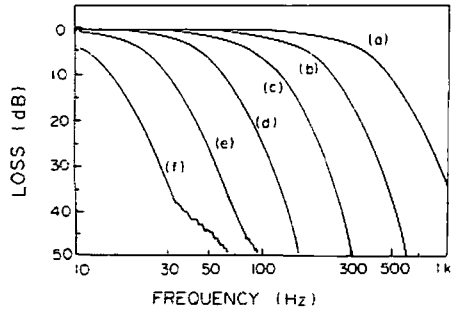

Fig. 12. Amplitude responses for LPF having six kinds of programmable cutoff frequencies.

when the output voltage goes down and $M5$ goes into saturation. The output stage has the capability to drive a 10 kΩ load in the 4.7 V peak-to-peak range. The operational amplifier characteristics are listed in Table II.

B. LSI Fabrication

A chip photomicrograph is shown in Fig. 9. Die size is 7.0×6.5 mm. The chip has been fabricated with a double-polysilicon CMOS process using 3.5 μm minimum gate length and 3.0 μm minimum line width. The smallest size unit capacitor for SCF's is 0.2 pF. The circuit can operate on a single 5 V power supply with 150 mW power consumption. The device, including 30 operational amplifiers, two comparators, a 396 bit RAM, and 500 digital gates, is mounted in a 28 pin dual-in-line package.

VII. Experimental Results

The amplitude response for the prefilter and the equalizer in a cascade form is shown in Fig. 10(a), where a 6 dB/oct emphasizing curve is realized. Fig. 10(b) gives the prefilter amplitude response which has an 8 kHz cutoff frequency and stopband attenuation of more than 50 dB.

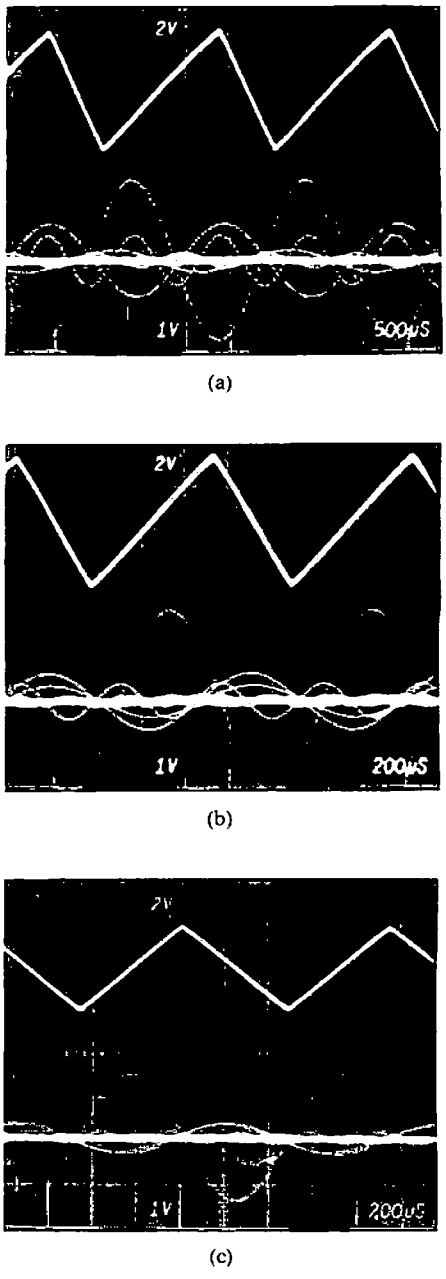

Fig. 13. Multiplexed BPF time responses. (a) 500 Hz sawtooth input. (b) 1100 Hz sawtooth input. (c) 1050 Hz triangular input.

Three BPF responses are shown in Fig. 11. They have the approximate Gaussian amplitude responses in the passband and the stopband attenuation of more than 40 dB.

Fig. 12 shows the LPF amplitude responses with six cutoff frequencies, 400, 200, 100, 50, 25, and 12.5 Hz indicated by (a)–(f), respectively. The stopband attenuation is more than 50 dB. The above measured filter responses are very close to the designed performance. This indicates that the crosstalk between multiplexed channels is almost negligible.

Fig. 13 shows the multiplexed BPF time responses which demonstrate spectrum analysis. The upper traces in Fig. 13(a) and (b) are 500 and 1100 Hz sawtooth input signals,

respectively. The lower traces are the multiplexed time responses of the BPF including the fundamental and second harmonic components. The upper trace in Fig. 13(c) is a 1050 Hz triangular input, and the lower trace shows the output with the fundamental and third harmonic components. The output offset difference among 20 channels is less than 5 mV.

Measured linearity error for the A/D converter is less than 1/4 LSB.

VIII. Conclusions

A single-chip speech spectrum analyzer was developed using 3.5 μm CMOS technology. This spectrum analyzer contains a 20-channel filter bank constructed with 6th-order BPF's and 8th-order LPF's, and an analog-to-digital interface consisting of a 9 bit A/D converter and a 396 bit buffer memory. A number of efficient SCF design techniques were introduced that allow for significantly reduced layout area, power dissipation, and output offsets. The developed LSI spectrum analyzer, together with CPU, the DP processor [16], and a large capacity memory chip, make it possible to construct a single board speech recognition system providing high-level recognition performance.

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