[See page 326 for Table 2]

SESSION IX: DEDICATED SIGNAL PROCESSORS

WPM 9.2: A Single-Chip 20-Channel Speech Spectrum Analyzer

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A SINGLE-CHIP speech-spectrum analyzer is one of the key elements that make it possible to construct small-size speech recognition systems with low-power consumption[1]. Furthermore, to achieve speech-recognition systems providing high-resolution rates, the chip is required to provide a high-resolution spectrum analysis and an analog-to-digital interface, as well as suppress noise, such as dc offsets.

This paper will present a single-chip speech spectrum analyzer satisfying these requirements. A classical filter bank approach is employed for spectrum analysis. Furthermore, switched capacitor filter (SCF) techniques are used to realize analog filter bank.

Figure 1 shows a block diagram of the speech spectrum analyzer LSI. A pre-filter, consisting of a 2nd-order RC active filter and a 10th-order switched capacitor lowpass filter (SC LPF), serving as an anti-aliasing filter, provides continuous-time signal sampling and also frequency reduction sampling from 200 to 18.18kHz. A filter bank consists of 22-channel bandpass filters (BPF) realized with 6th-order SCFs, whose calculated amplitude responses are listed in Table I. Twenty channels are assigned for spectrum analysis and the remaining two channels are used to observe dc offsets. The filter bank outputs are full-wave rectified and their dc components are filtered by a 22-channel lowpass filter bank realized with 8th-order SCFs. The LPF's cutoff frequencies can be selected from six frequencies – 12.5, 25, 50, 100, 200, and 400Hz – through the CPU control, taking into account the LPF output integration interval. An ADC using a capacitor array has 9b resolution. The A/D converter outputs are stored in a buffer memory, and can be asychronously read by the CPU.

Since both the bandpass and lowpass filter banks contain 308th-order filters as a whole, SCF design techniques to reduce chip area and power consumption are inherently required. For this purpose, the sampling frequencies for the filter banks are reduced from 200kHz to 18.8kHz, and a multiplexed SCF technique[2] is employed. By using an operational amplifier (opamp) shared by 22-channel filters, both the bandpass and lowpass filter banks can be synthesized using only 14 opamps. The opamps are required to operate on a 400kHz clock rate with low power consumption. Those requirements are satisfied by employing a 3.5μm CMOS process. The pertinent opamp schematic and design characteristics are shown in Figure 2 and Table II, respectively. From these design approaches, filter bank area and power consumption are reduced to 4.5mm x 5.1mm and 74mW, respectively.

To achieve 9b precision performance, noise, such as dc offsets produced in SCFs, must be suppressed. Particularly, dc offsets among 20-channel BPFs become large, because the dc offsets caused by the feedthrough are mainly determined by ratios of SCF capacitances and the parasitic capacitances of MOS switches[3]. The SCF capacitances usually differ for each channel. Furthermore, it is difficult to cancel those different dc offsets caused in the multiplexed SCFs with simple circuits. A useful approach to suppressing these dc offsets is to make dc offsets uniform for each channel. For this purpose, in the developed LSI, the same capacitances are used for all multiplexed BPFs. Equivalent capacitance ratios are realized using resistive dividers, as shown in Figure 3. The resistive dividers consist of 198 unit resistors to achieve the necessary precision. The resistance ratios are essential to minimize the mean square errors for equivalent capacitance ratios. Additional capacitors ($C_{a1} \sim C_{a4}$) in Figure 3 are utilized to reduce variation in the dc offsets, due to differing source impedances[3]. Furthermore, in the BPF circuits, a 2nd-order section having its transmission zero at dc is assigned to the output stage. These techniques serve to reduce the dc offsets. The measured dc offsets, after being suppressed by a coupling capacitor C_B, as shown in Figure 3, are less than 5mV.

In the lowpass filter bank, two types of transfer functions are used for low-band channels ($1 \sim 10$) and high-band channels ($11 \sim 20$), respectively. Therefore, the dc offsets can be monitored by using two dummy channels, and are cancelled in the CPU.

The fabricated LSI, shown in Figure 4, is mounted on a 28 pin dual-in-line package. It operates on a +5V power supply with 150mW power consumption. The die size is 7.0mm x 6.5mm using a 3.5μm CMOS process. Examples of the measured BPF's amplitude responses are shown in Figure 5.

Channel Number	*Center Frequency (Hz)*	*–3dB Bandwidth (Hz)*
1	485	270
2	730	280
3	980	280
4	1220	260
·	·	·
·	·	·
·	·	·
15	3900	280
16	4145	290
17	4520	540
18	5005	510
19	5735	990
20	6700	1000
21	Dummy	–
22	Dummy	–

TABLE 1–Bandpass filter responses.

[1] Lin, L.T., et. al., "A Monolithic Audio Spectrum Analyzer for Speech Recognition Systems", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 272-273; Feb., 1982.

[2] Bosshart, P.W., "A Multiplexed Switched Capacitor Filter Bank", *IEEE J. Solid-State Circuits*, Vol. SC-15, p. 939-945; Dec., 1980.

[3] Yen, R.C. and Gray, P.R., "A MOS Switched-Capacitor Instrumentation Amplifier", *IEEE J. Solid-State Circuits*, Vol. SC-17, p. 1008-1013; Dec., 1982.

[4] Iwata, T., et. al., "A Speech Recognition Processor", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 120-121; Feb., 1983.

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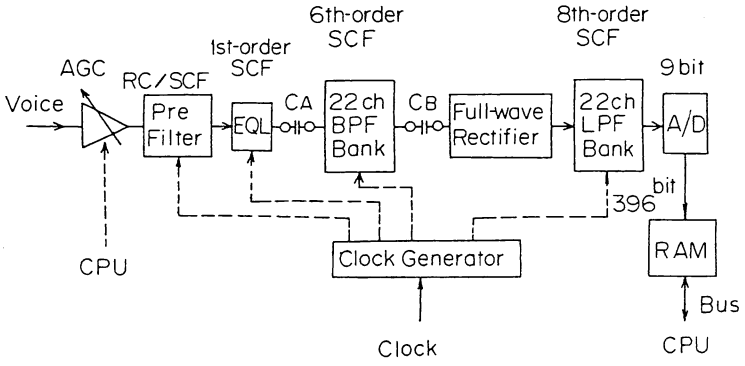

FIGURE 1—Speech spectrum analyzer LSI block diagram.

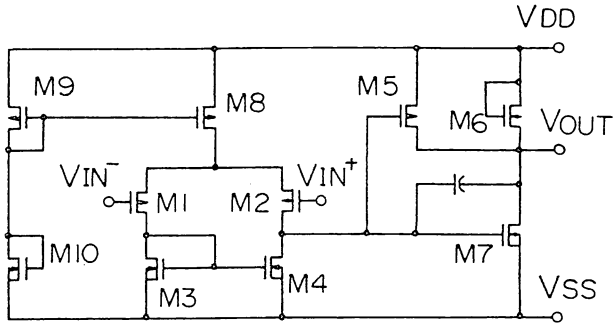

FIGURE 2—Operational amplifier schematic.

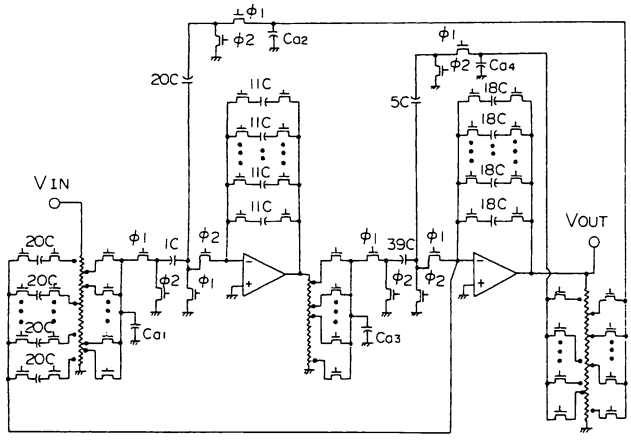

FIGURE 3—Multiplexed 2nd-order SCF schematic.

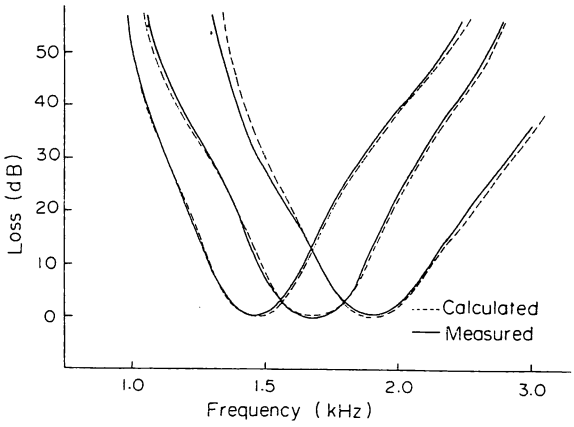

FIGURE 5—Examples of measured bandpass filter responses.

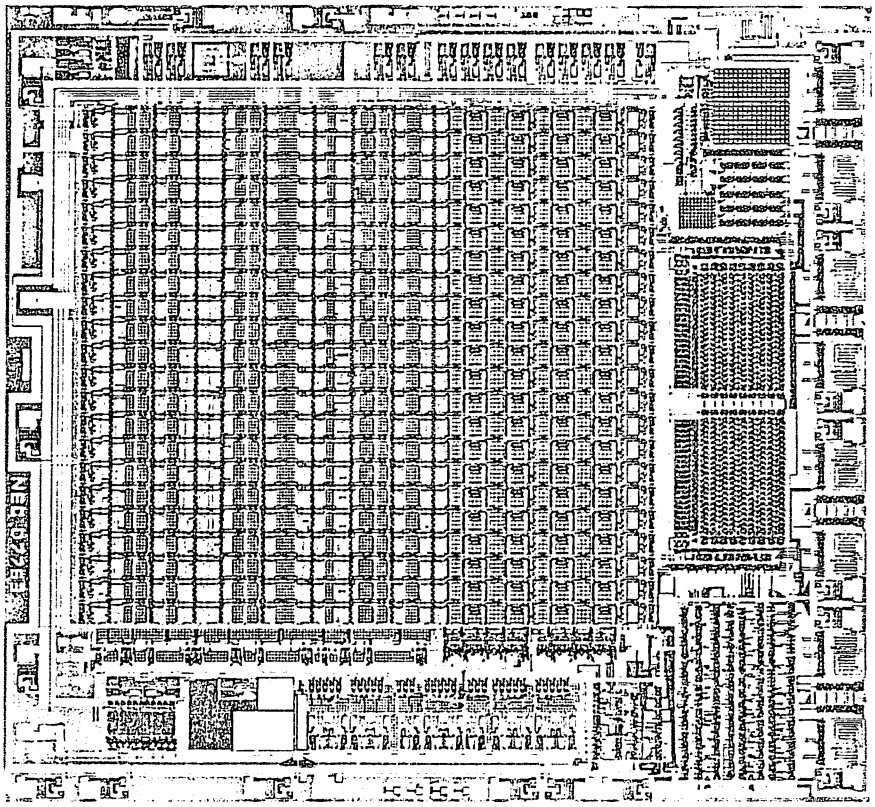

FIGURE 4—Chip microphotograph.