SESSION III: SAMPLED-DATA ANALOG CIRCUITS

WAM 3.4; An Oversampling ADC Macrocell with Rail-to-Rail Input Voltage Capability

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AN OVERSAMPLING ADC, which achieves a result equivalent to 14b resolution and less than −80dB harmonic distortion at almost 5Vp-p input signal amplitude, has been realized in a single 5V 1.5μm CMOS IC.

Many programs have been pursued on oversampling ADCs for telecommunication applications, such as digital codecs and high speed modems[1−4] Preferred characteristics for a general purpose ADC macrocell for future VLSIs are: *1*—linear A-to-D conversion characteristics, *2*—small chip area, *3*—low power dissipation, *4*—large input voltage range with low power supply voltage to decrease device noise effects, and *5*—lower oversampling data bit rate to decrease not only digital hardware, but also to decrease power dissipation. Earlier designs require a greater than 3Mb/s data bit rate to achieve 14b resolution. However, with a proposed oversampling ADC it is possible to achieve a 1Mb/s data rate.

The proposed design is a 1st-order predictive encoder with 1st-order noise shaping[5]. The structure has a different signal path for loop stabilization than its predecessors. The predictor function is performed digitally. The problem of harmonic distortion generated by a non-ideal D-to-A converter, which reconstruct the feedback prediction signal, has been decreased by using a balanced configuration and decreasing the internal analog signal swing, which is inherent in the configuration. The basic circuit structure, shown in Figure 1, has been designed for voiceband telecommunication applications with 14b accuracy. An analysis indicates that 1MHz sampling and a 6b DAC for the predictor is adequate for this structure. The converter consists of a balanced operational amplifier for analog integration, two 5b capacitor arrays, instead of a 6b capacitor array, with an extra unit capacitor for converting positive and negative data to analog values, a pair of input sampling capacitors, a balanced comparator, a 5b up/down counter with a polarity flip-flop as a predictor, polarity control switch and small control logic.

In operation, the incoming signal is sampled on the sampling capacitor array pair alternately at every half cycle to accomplish conversion from a single ended-signal to a balanced signal. The sampled signal and predicted value in the up/down counter are directly subtracted by the capacitor array. The difference, which is less than 1LSB for the 6b DAC, and an extra 1LSB signal, for loop stabilization, are integrated in the integrating capacitor. The integrated voltage is tested by the comparator. The tested result is fed to the count control logic and serves as a single bit differential output code. The output single bit code can be processed by a digital filter with one extra integrator.

The circuit structure has more desirable features for CMOS implementations. The analog voltage to be processed is only the output of the integrating amplifier. This voltage is a summation of the imcoming signal and predicted value difference, which is less than 1LSB for the predictor, and an extra 1LSB, which is fed by the comparator directly for loop stabilization. Therefore, the internal analog voltage swing is limited to about two LSBs for the predictor. This feature eliminates amplifier slewing requirements and distortion generated by the amplifier and adds nearly rail-to-rail input voltage handling capability without signal attenuation. This feature also allows the circuit the time for an offset cancelling cycle and eliminates low frequency 1/f noise, which is often harmful to analog MOS circuits. On the contrary, the high frequency noise component may be helpful as a dither signal to the converter. The balanced signal feature has an advantage in regard to excellent power supply rejection characteristic and elimination of even-order harmonic distortion caused by the capacitor array nonlinearity with little area increase penalty.

Device evaluation has been carried out thoroughly in the digital domain using a fast Fourier transform to eliminate distortion appearing when a DAC is employed for spectrum evaluation. The signal to total distortion in the signal band has been plotted in Figure 2 for 1kHz and 1.25kHz signals. Here, maximum peak-to-peak signal amplitude was set at 4.9V at 3.2dB. The S/D performance shows 14b accuracy. Signal tracking performance was plotted in Figure 3 for the same frequency as in Figure 2. An output spectrum for the 1.25kHz 3dB signal as shown in Figure 4. The 2nd and 3rd harmonic distortions are about 83dB less than the fundamental signal. The device worked down to 4V power supply voltage without any performance degradation. The maximum operating speed was 6MHz, thanks to the small internal voltage swing.

A photo of the chip is shown in Figure 5. The active area is 1.5mm x 0.8mm. Unit capacitance is 0.2pF. Measured characteristics are summarized in Table 1.

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[1] Wooley, B.A. and Henry, J.L., "An Integrated Per-Channel PCM Encoder Based on Interpolation", *IEEE Journal of Solid-State Circuits*, Vol. SC-15, p. 14-20; 1979.

[2] Schmid, E. and Reisinger, J., "High Performance Oversampling A/D-Converter for Digital Signal Processing Applications", *ESSCIRC*, p. 201-204; 1984.

[3] Yamakido, K., et. al., "A Voiceband 15b Interpolative Converter Chip Set", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 180-181; Feb., 1986.

[4] Hayashi, T., et. al., "A Mutlistage Delta-Sigma Modulator Without Double Integration Loop", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 182-183; Feb., 1986.

[5] Yukawa, A., et. al., "An Oversampling A-to-D Converter Structure for VLSI Digital Codecs", *ICASSP Proceedings*, p. 1400-1403; 1985.

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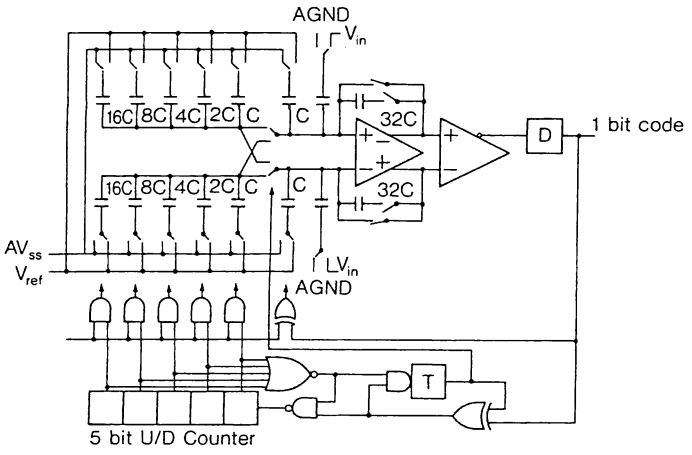

FIGURE 1—A-to-D converter schematic.

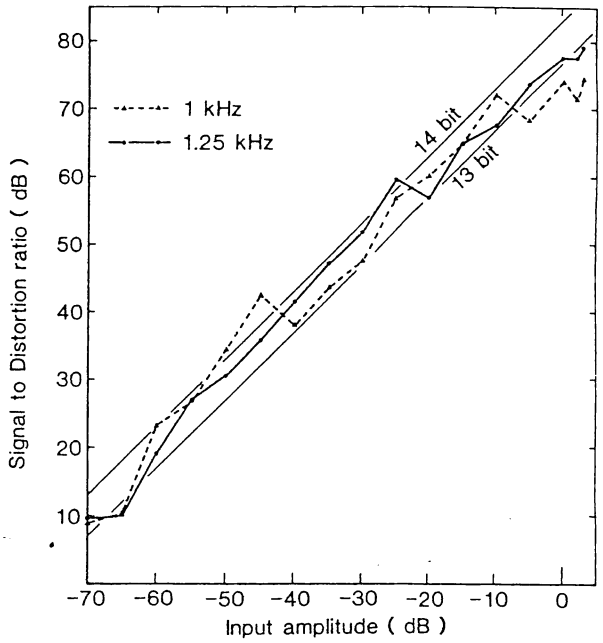

FIGURE 2—Signal to total distortion characteristics.

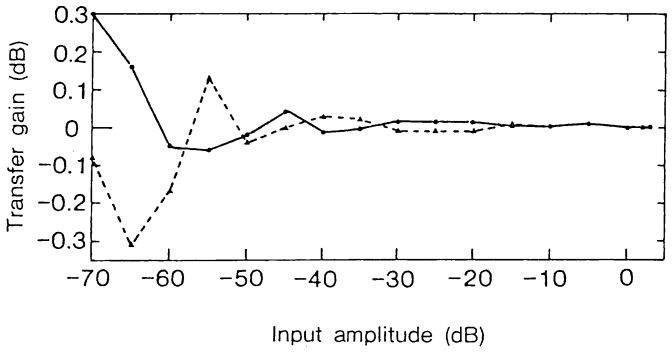

FIGURE 3—Gain tracking performance.

Power dissipation

Amplifier	5mW
Comparator	0.7mW
Logic	2.1mW

Characteristics

Accuracy	14b
2nd harmonic	−83dB
3rd harmonic	−83dB
PSRR	>70dB
Active area	1.5mm×0.8mm

TABLE 1—Measured performance.

[See page 335 for Figure 5.]

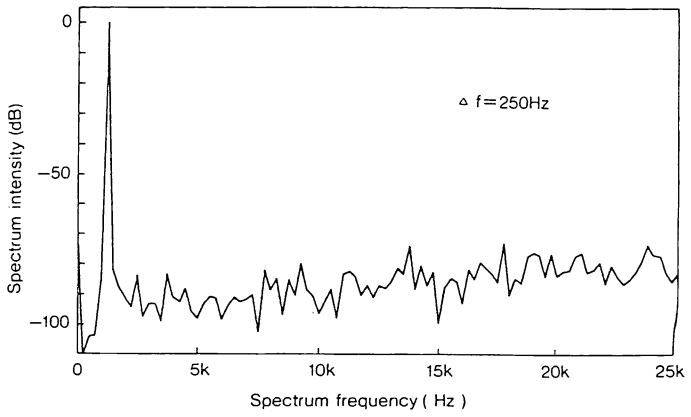

FIGURE 4—Output spectrum for 1.25kHz 4.7 Vp-p sinusoid.

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TABLE 1—Typical performance, 25C, ± 5V supplies: *a*—ADC; *b*—input sample/hold and programmable amplifier function; *c*—voltage reference; *d*—overall chip.

Integral nonlinearity after cal	0.4LSB @ 12b
Input offset voltage	0.3mV
Conversion time (includes gain, S/H)	
8b, 1x gain	18μs
13b, 1x gain	25μs
8b. 8x gain	21μs
13b, 8x gain	28μs
Max. V_{ref} value	3.2V

(a)

Input offset voltage	0.1mV
CMRR (dc)	>100dB
PSRR (dc)	76dB

(b)

Nominal output value	2.500V
Drift, 0-70C	± 18ppm
PSRR	85dB
Max output current	3mA
Rout	0.15Ω
Thermometer output sensitivity	5mV/degC

(c)

Power dissipation, active	250mW
Power dissipation, power down	1mW
System gain accuracy (external V_{ref})	0.04%
Die size	255 x 272mil
Technology	3μm, 2 poly CMOS
Number of transistors	25,000

(d)

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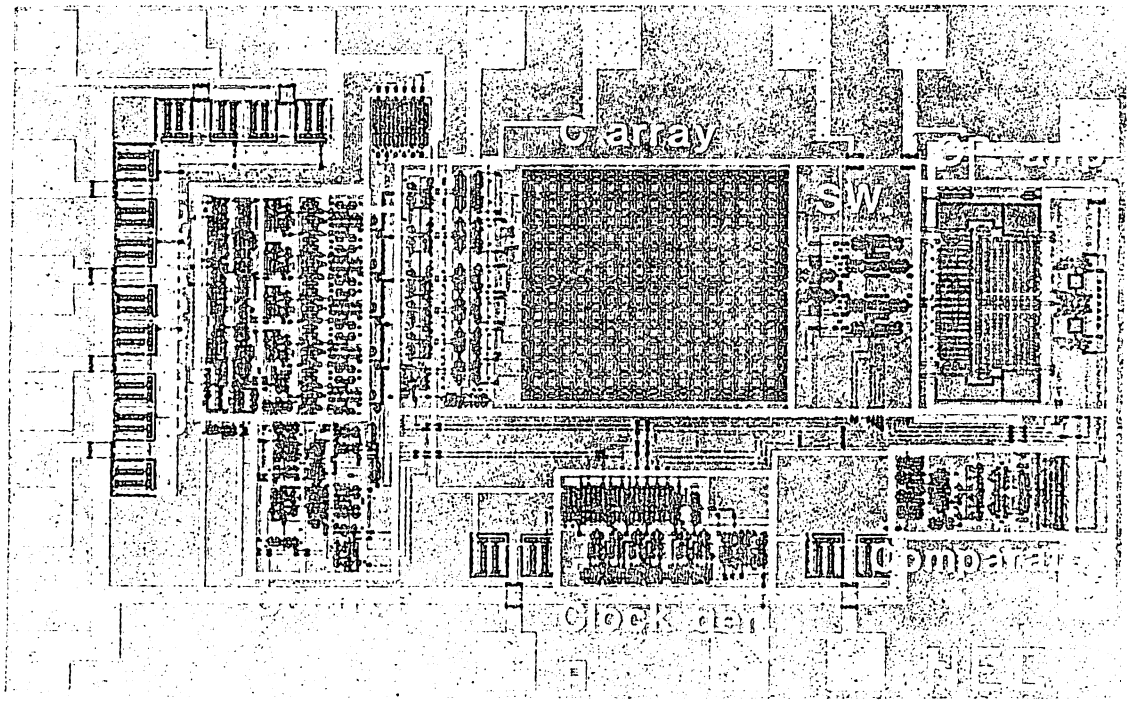

FIGURE 5—Chip photomicrograph.